TCA9535 Low-Voltage 16-Bit I²C and SMBus Low-Power I/O Expander with Interrupt Output and Configuration Registers

1 Features

- I²C to Parallel Port Expander
- Wide Power Supply Voltage Range of 1.65 V to 5 V
- Low Standby-Current Consumption
- Open-Drain Active-Low Interrupt Output
- 5-V Tolerant I/O Ports
- 400-kHz Fast I²C Bus
- Polarity Inversion Register
- Address by Three Hardware Address Pins for Use of up to Eight Devices
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics (For Example, Gaming Consoles)
- Industrial Automation
- Products With GPIO-Limited Processors

3 Description

The TCA9535 is a 24-pin device that provides 16 bits of general purpose parallel input and output (I/O) expansion for the two-line bidirectional I²C bus or (SMBus) protocol. The device can operate with a power supply voltage ranging from 1.65 V to 5.5 V.

The TCA9535 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits.

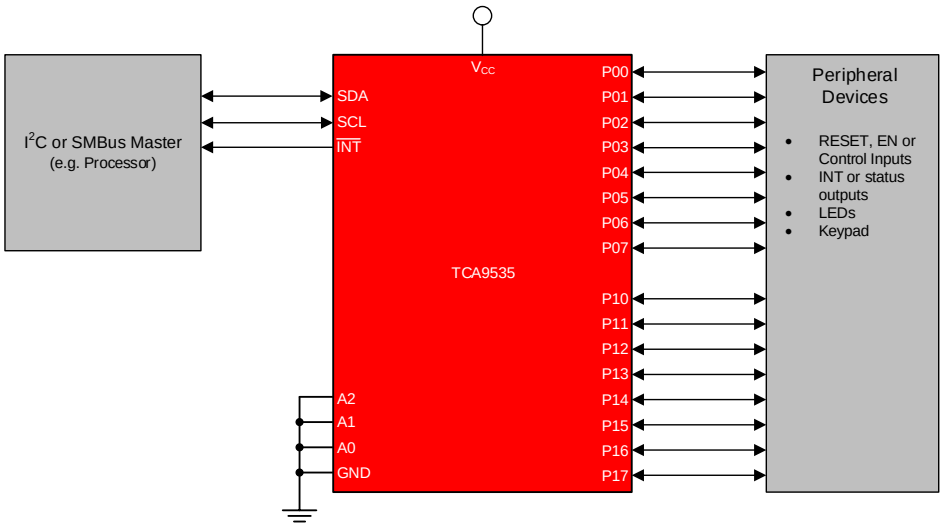
The TCA9535 is identical to the TCA9555, except that the TCA9535 does not include the internal I/O pull-up resistor, which requires pull-ups and pull-downs on unused I/O pins when configured as an input and undriven.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA9535	TSSOP (24)	7.80 mm x 4.40 mm
	SSOP (24)	6.20 mm x 5.30 mm
	WQFN (24)	4.00 mm x 4.00 mm
	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2016) to Revision D — **Page**

- Added DB package ... 1

Changes from Revision B (August 2015) to Revision C — **Page**

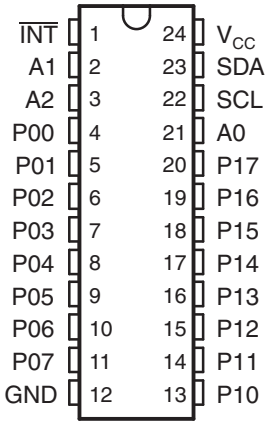
- Added RGE package. ... 1
- Added I_{OL} for different T_j ... 4
- Deleted ΔI_{CC} spec from the Electrical Characteristics table, added ΔI_{CC} typical characteristics graph ... 5
- Changed I_{CC} standby into different input states, with increased maximums ... 6
- Changed C_{io} maximum ... 6
- Deleted ΔI_{CC} spec from the Electrical Characteristics table, added ΔI_{CC} typical characteristics graph ... 6

Changes from Revision A (September 2009) to Revision B — **Page**

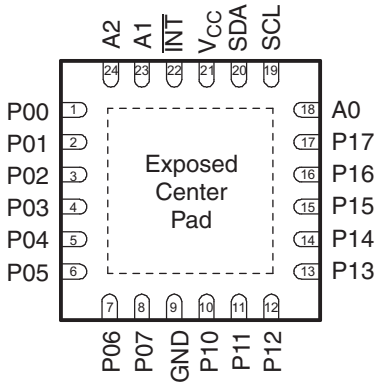
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DB, PW Package
24-Pin TSSOP
Top View



RTW, RGE Package
24-Pin WQFN, VQFN
Top View



The exposed center pad, if used, must be connected as a secondary ground or left electrically open.

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	DB, PW	RTW, RGE		
A0	21	18	Input	Address input 0. Connect directly to V_{CC} or ground
A1	2	23	Input	Address input 1. Connect directly to V_{CC} or ground
A2	3	24	Input	Address input 2. Connect directly to V_{CC} or ground
GND	12	9	—	Ground
$\overline{INT}$	1	22	Output	Interrupt output. Connect to V_{CC} through an external pull-up resistor
P00(1)	4	1	I/O	P-port I/O. Push-pull design structure. At power on, P00 is configured as an input
P01(1)	5	2	I/O	P-port I/O. Push-pull design structure. At power on, P01 is configured as an input
P02(1)	6	3	I/O	P-port I/O. Push-pull design structure. At power on, P02 is configured as an input
P03(1)	7	4	I/O	P-port I/O. Push-pull design structure. At power on, P03 is configured as an input
P04(1)	8	5	I/O	P-port I/O. Push-pull design structure. At power on, P04 is configured as an input
P05(1)	9	6	I/O	P-port I/O. Push-pull design structure. At power on, P05 is configured as an input
P06(1)	10	7	I/O	P-port I/O. Push-pull design structure. At power on, P06 is configured as an input
P07(1)	11	8	I/O	P-port I/O. Push-pull design structure. At power on, P07 is configured as an input
P10(1)	13	10	I/O	P-port I/O. Push-pull design structure. At power on, P10 is configured as an input
P11(1)	14	11	I/O	P-port I/O. Push-pull design structure. At power on, P11 is configured as an input
P12(1)	15	12	I/O	P-port I/O. Push-pull design structure. At power on, P12 is configured as an input
P13(1)	16	13	I/O	P-port I/O. Push-pull design structure. At power on, P13 is configured as an input
P14(1)	17	14	I/O	P-port I/O. Push-pull design structure. At power on, P14 is configured as an input
P15(1)	18	15	I/O	P-port I/O. Push-pull design structure. At power on, P15 is configured as an input
P16(1)	19	16	I/O	P-port I/O. Push-pull design structure. At power on, P16 is configured as an input
P17(1)	20	17	I/O	P-port I/O. Push-pull design structure. At power on, P17 is configured as an input
SCL	22	19	Input	Serial clock bus. Connect to V_{CC} through a pull-up resistor
SDA	23	20	Input	Serial data bus. Connect to V_{CC} through a pull-up resistor
V_{CC}	24	21	—	Supply voltage

(1) If port is unused, it must be tied to either V_{CC} or GND through a resistor of moderate value (about 10 kΩ)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6	V
V_I	Input voltage(2)		–0.5	6	V
V_O	Output voltage(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input-output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	mA
$T_{j(MAX)}$	Maximum junction temperature			100	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA		0.7 × V_{CC}	V_{CC} (1)	V
		A2–A0, P07–P00, P17–P10		0.7 × V_{CC}	5.5	V
V_{IL}	Low-level input voltage	SCL, SDA, A2–A0, P07–P00, P17–P10		–0.5	0.3 × V_{CC}	V
I_{OH}	High-level output current	P07–P00, P17–P10			–10	mA
I_{OL}	Low-level output current(2)	P07–P00, P17–P10	$T_j \le 65°C$		25	mA
			$T_j \le 85°C$		18	
			$T_j \le 100°C$		11	
I_{OL}	Low-level output current(2)	$\overline{INT}$, SDA	$T_j \le 85°C$		6	mA
			$T_j \le 100°C$		3.5	
T_A	Operating free-air temperature			–40	85	°C

(1) For voltages applied above V_{CC}, an increase in I_{CC} results.
(2) The values shown apply to specific junction temperatures, which depend on the $R_{\theta JA}$ of the package used. See the *Calculating Junction Temperature and Power Dissipation* section on how to calculate the junction temperature.

6.4 Thermal Information

THERMAL METRIC[1]		TCA9535				UNIT
		PW (TSSOP)	DB (SSOP)	RTW (WQFN)	RGE (VQFN)	
		24 PINS	24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.8	92.9	43.6	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	53.5	46.2	58.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	50.4	22.1	27.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	21.9	1.5	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.3	50.1	22.2	27.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	10.7	15.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage		I_I = –18 mA	1.65 V to 5.5 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising		V_I = V_{CC} or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		V_I = V_{CC} or GND, I_O = 0		0.75	1		V
V_{OH}	P-port high-level output voltage[2]		I_{OH} = –8 mA	1.65 V	1.2			V
				2.3 V	1.8			
				3 V	2.6			
				4.75 V	4.1			
			I_{OH} = –10 mA	1.65 V	1			
				2.3 V	1.7			
				3 V	2.5			
				4.75 V	4			
I_{OL}	Low-level output current	SDA	V_{OL} = 0.4 V	1.65 V to 5.5 V	3			mA
		P port[3]	V_{OL} = 0.5 V	1.65 V to 5.5 V	8			
			V_{OL} = 0.7 V	1.65 V to 5.5 V	10			
		$\overline{INT}$	V_{OL} = 0.4 V	1.65 V to 5.5 V	3			
I_I	Input leakage current	SCL, SDA Input leakage	V_I = V_{CC} or GND	1.65 V to 5.5 V			±1	µA
		A2–A0 Input leakage	V_I = V_{CC} or GND	1.65 V to 5.5 V			±1	
I_{IH}	Input high leakage current	P port	V_I = V_{CC}	1.65 V to 5.5 V			1	µA
I_{IL}	Input low leakage current	P port	V_I = GND	1.65 V to 5.5 V			–1	µA

(1) All typical values are at nominal supply voltage (1.8-, 2.5-, 3.3-, or 5-V V_{CC}) and T_A = 25°C.
(2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
I_{CC}	Quiescent current	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, f_{SCL} = 400 kHz, No load	5.5 V		22	40	µA
				3.6 V		11	30	
				2.7 V		8	19	
				1.95 V		5	11	
		Standby mode	$V_I = V_{CC}$, $I_O = 0$, I/O = inputs, f_{SCL} = 0 kHz, No load	5.5 V		1.5	3.9	
				3.6 V		0.9	2.2	
				2.7 V		0.6	1.8	
				1.95 V		0.6	1.5	
			V_I = GND, $I_O = 0$, I/O = inputs, f_{SCL} = 0 kHz, No load	5.5 V		1.5	8.7	
				3.6 V		0.9	4	
				2.7 V		0.6	3	
				1.95 V		0.4	2.2	
C_I	Input capacitance	SCL	$V_I = V_{CC}$ or GND	1.65 V to 5.5 V		3	8	pF
C_{io}	Input-output pin capacitance	SDA	$V_{IO} = V_{CC}$ or GND	1.65 V to 5.5 V		3	9.5	pF
		P port	$V_{IO} = V_{CC}$ or GND	1.65 V to 5.5 V		3.7	9.5	

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 20)

			MIN	MAX	UNIT
I²C BUS—STANDARD MODE					
f_{scl}	I²C clock frequency		0	100	kHz
t_{sch}	I²C clock high time		4		µs
t_{scl}	I²C clock low time		4.7		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between stop and start		4.7		µs
t_{sts}	I²C start or repeated start condition setup		4.7		µs
t_{sth}	I²C start or repeated start condition hold		4		µs
t_{sps}	I²C stop condition setup		4		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs
C_b	I²C bus capacitive load			400	pF
I²C BUS—FAST MODE					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns

I^2C Interface Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 20)

			MIN	MAX	UNIT
t_{icf}	I^2C input fall time		20 × (V_{CC} / 5.5 V)	300	ns
t_{ocf}	I^2C output fall time	10-pF to 400-pF bus	20 × (V_{CC} / 5.5 V)	300	ns
t_{buf}	I^2C bus free time between stop and start		1.3		µs
t_{sts}	I^2C start or repeated start condition setup		0.6		µs
t_{sth}	I^2C start or repeated start condition hold		0.6		µs
t_{sps}	I^2C stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs
C_b	I^2C bus capacitive load			400	pF

6.7 Switching Characteristics

over recommended operating free-air temperature range, C_L ≤ 100 pF (unless otherwise noted) (see Figure 20 and Figure 21)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs
t_{pv}	Output data valid; For V_{CC} = 2.3 V–5.5 V	SCL	P port		200	ns
	Output data valid; For V_{CC} = 1.65 V–2.3 V				300	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

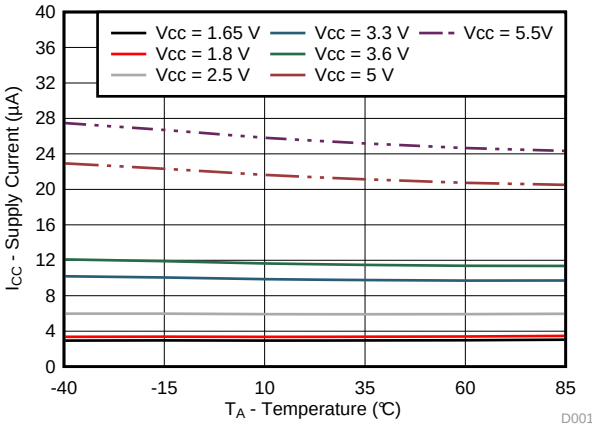


Figure 1. Supply Current vs Temperature for Different Supply Voltage (V_{CC})

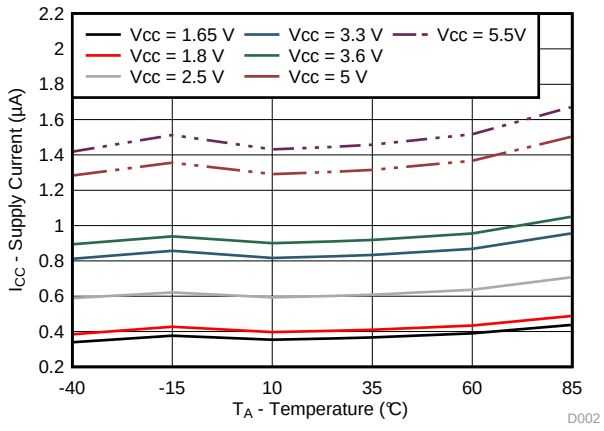


Figure 2. Standby Supply Current vs Temperature for Different Supply Voltage (V_{CC})

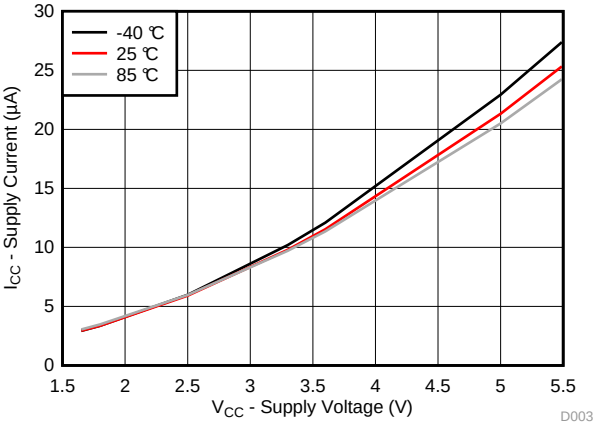


Figure 3. Supply Current vs Supply Voltage for Different Temperature (T_A)

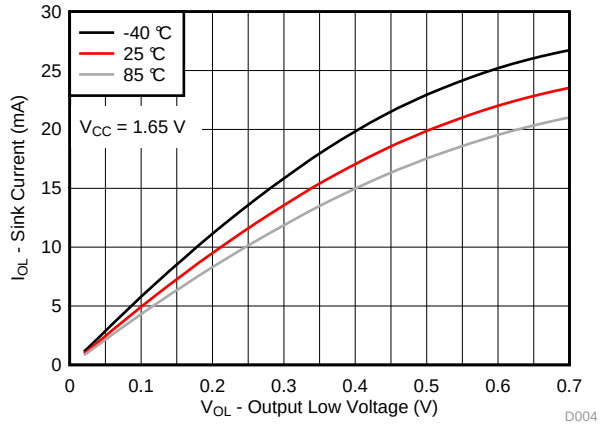


Figure 4. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

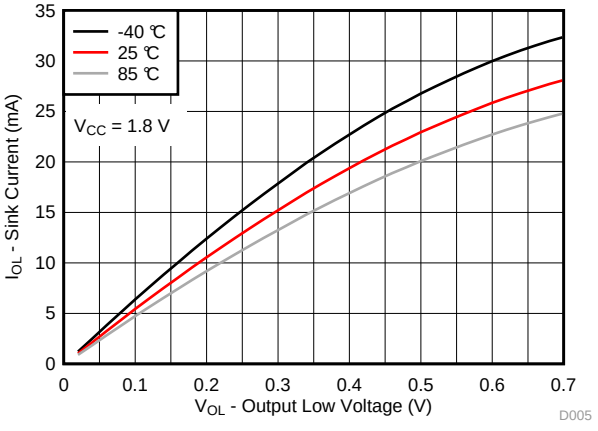


Figure 5. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

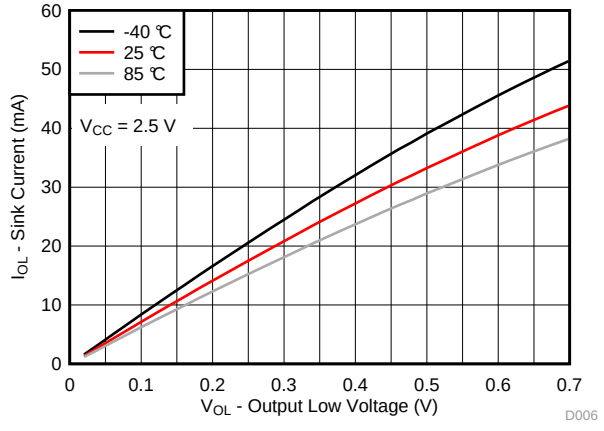


Figure 6. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

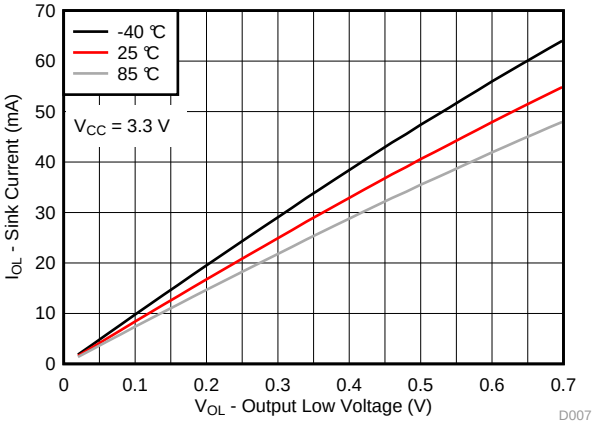


Figure 7. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

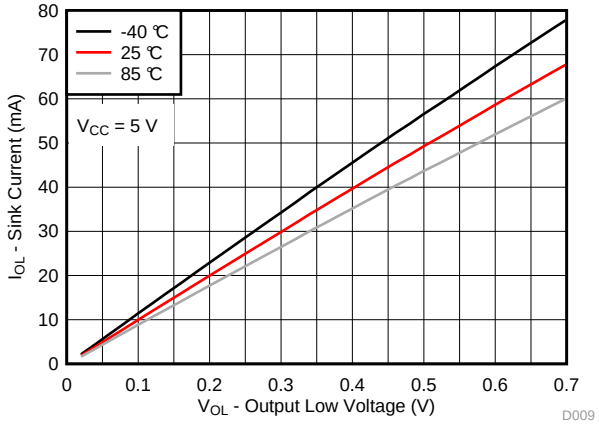


Figure 8. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5 V

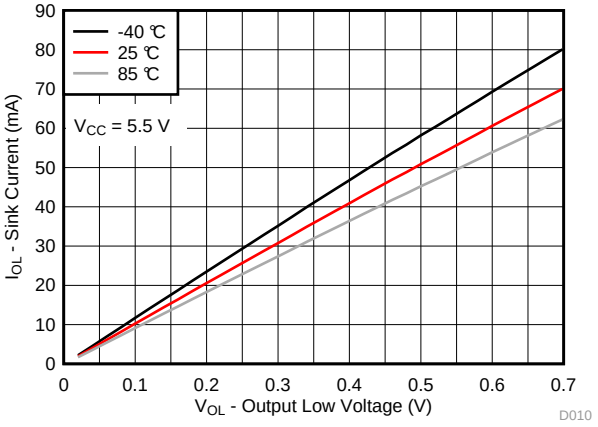


Figure 9. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

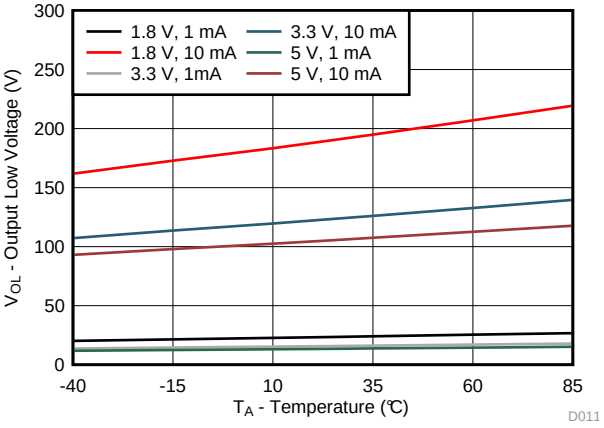


Figure 10. I/O Low Voltage vs Temperature for Different V_{CC} and I_{OL}

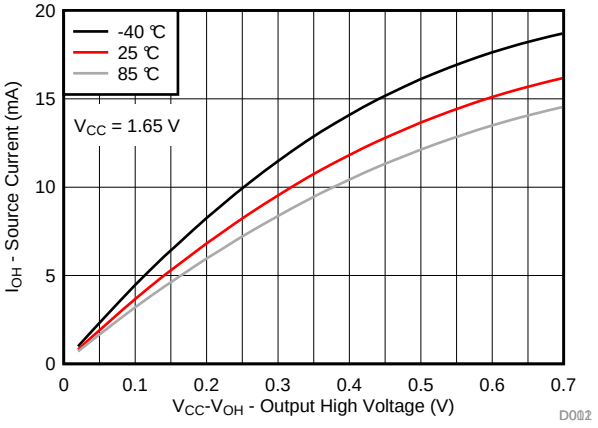


Figure 11. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

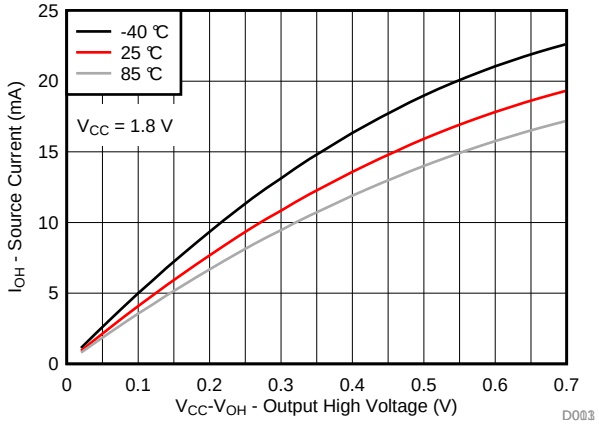


Figure 12. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

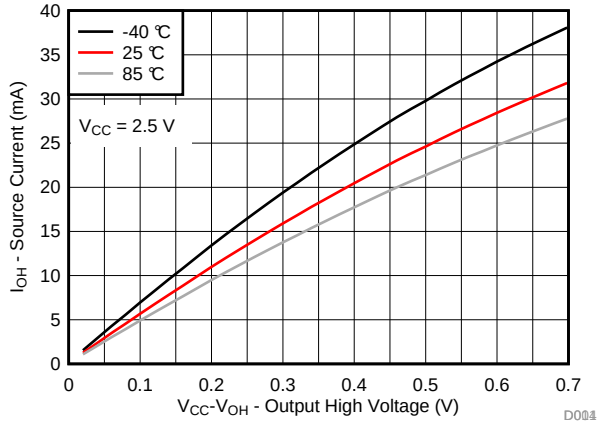


Figure 13. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

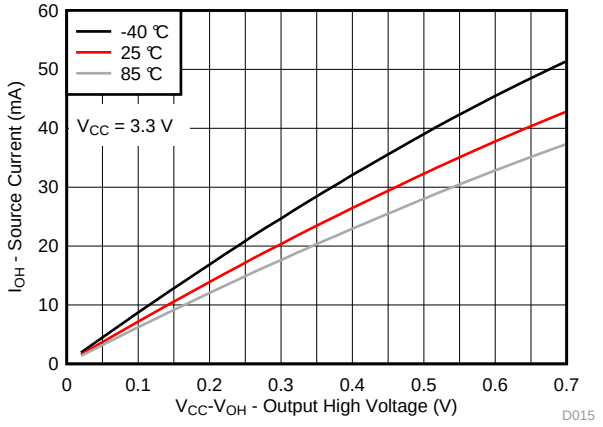


Figure 14. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

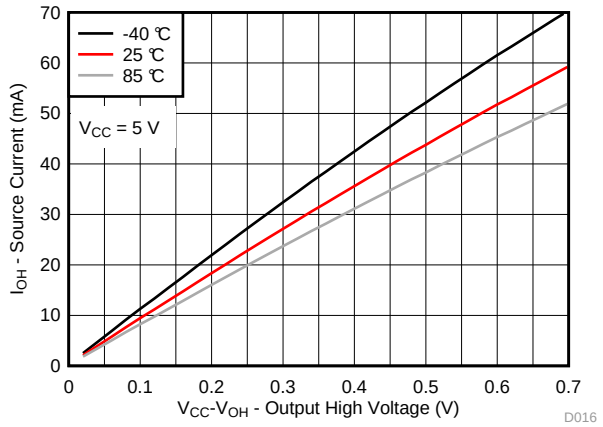


Figure 15. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5 V

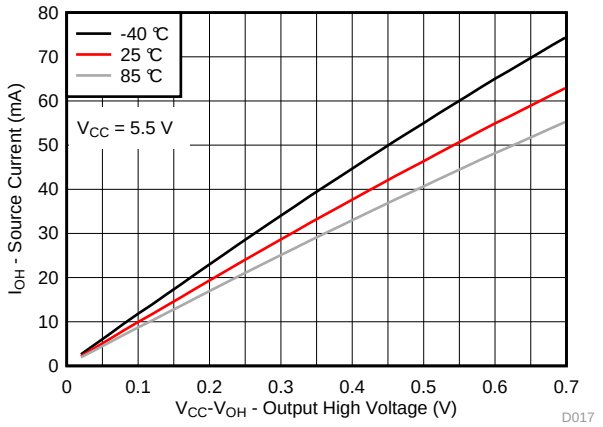


Figure 16. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

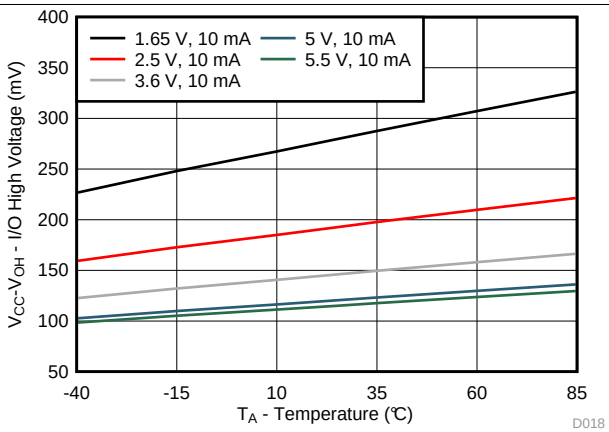


Figure 17. V_{CC} – V_{OH} Voltage vs Temperature for Different V_{CC}

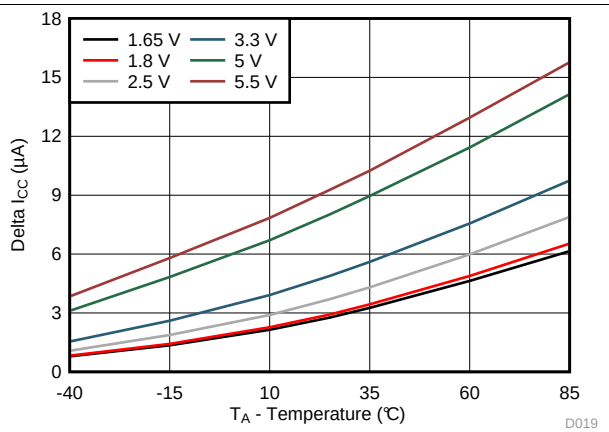
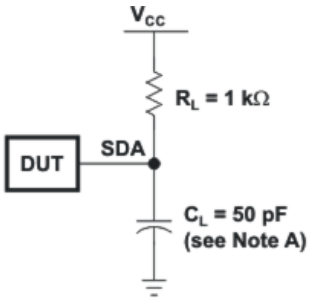
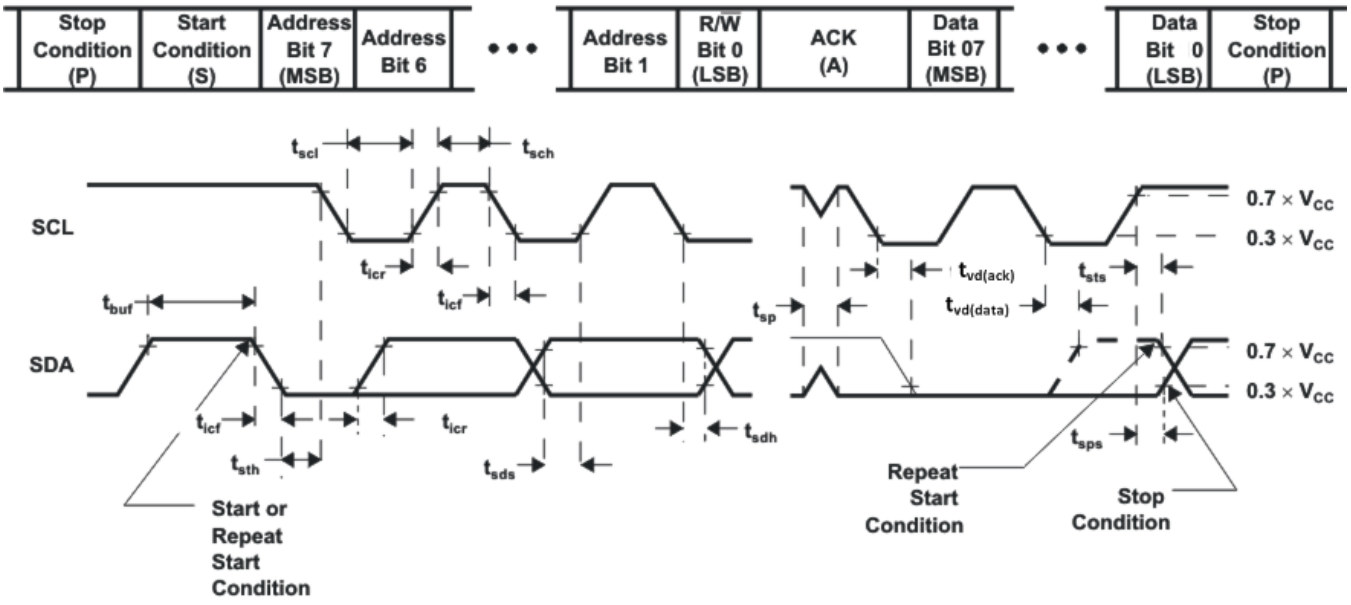


Figure 18. Δ I_{CC} vs Temperature for Different V_{CC} (V_I = V_{CC} – 0.6 V)

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

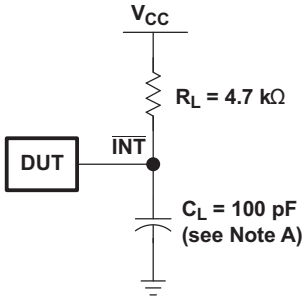
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

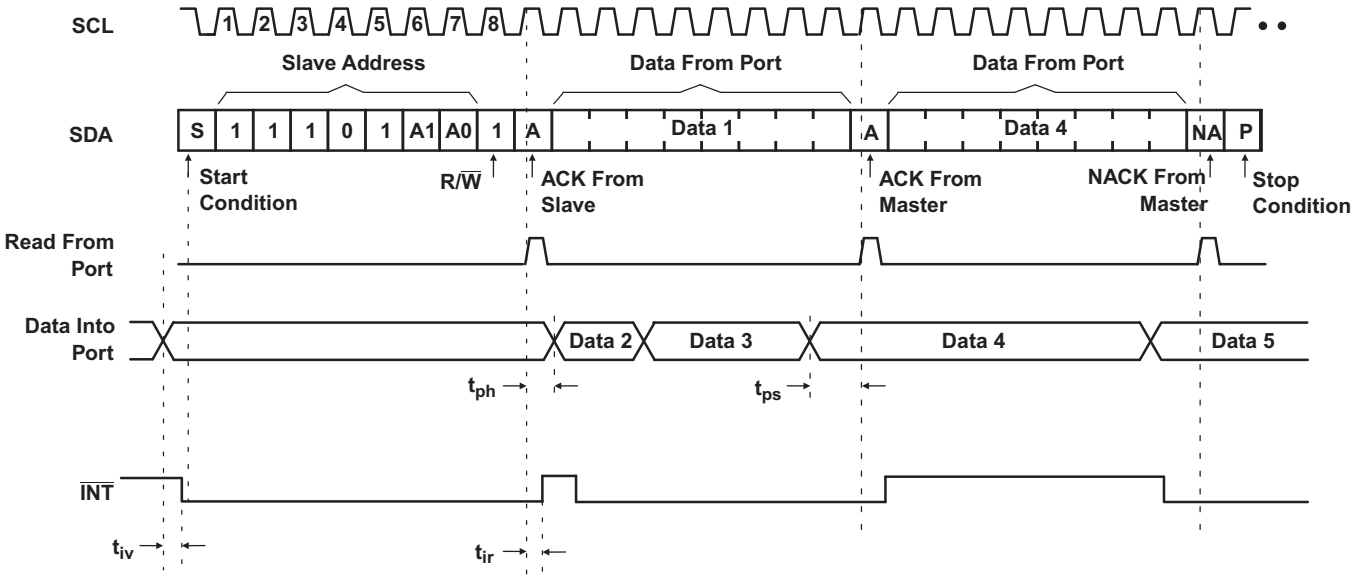
C. All parameters and waveforms are not applicable to all devices.

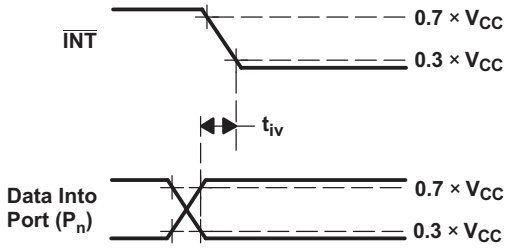
Figure 19. I^2C Interface Load Circuit and Voltage Waveforms

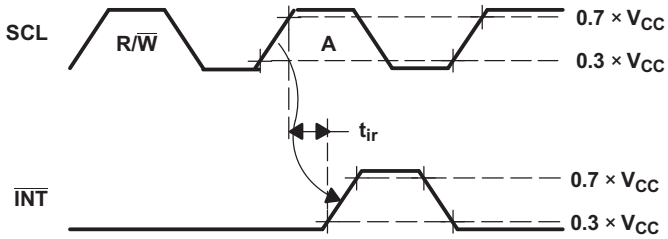
Parameter Measurement Information (continued)



Interupt Load Configuration







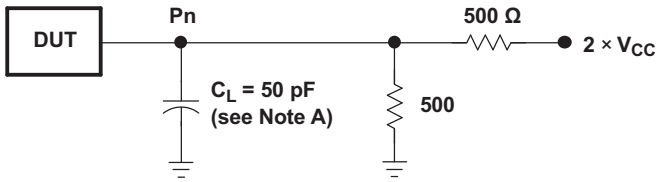
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

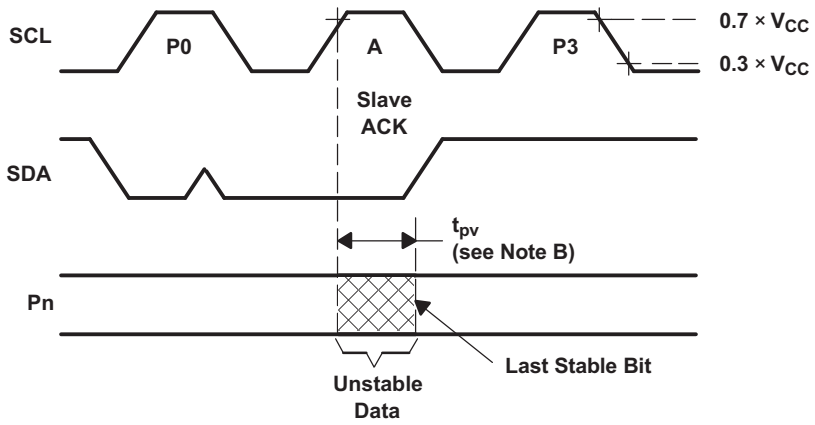
C. All parameters and waveforms are not applicable to all devices.

Figure 20. Interrupt Load Circuit and Voltage Waveforms

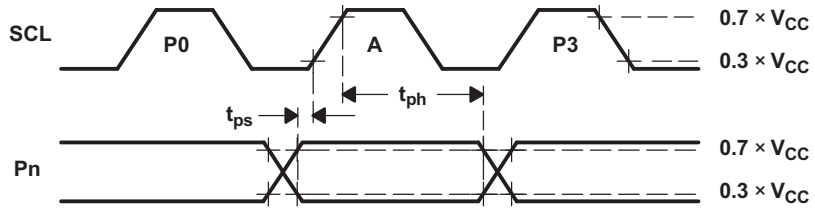
Parameter Measurement Information (continued)



P-Port Load Configuration



Write Mode (R/$\overline{W}$ = 0)



Read Mode (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 21. P-Port Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TCA9535 device is a 16-bit I/O expander for the I^2C bus and is designed for 1.65-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface.

The TCA9535 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding Input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The TCA9535 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

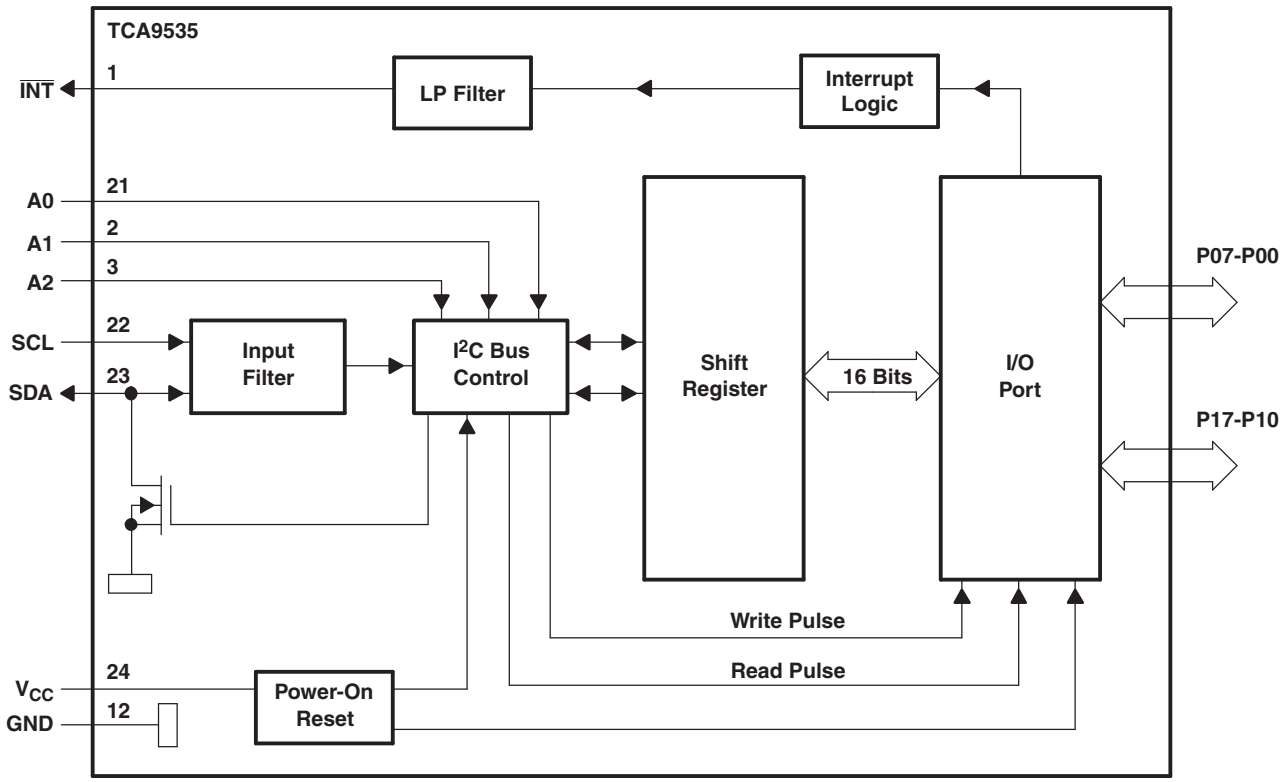
$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA9535 can remain a simple slave device.

The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption.

The TCA9535 device is similar to the PCA9555, except for the removal of the internal I/O pull-up resistor, which greatly reduces power consumption when the I/Os are held low. The TCA9535 is equivalent to the PCA9535 with lower voltage support (down to V_{CC} = 1.65 V), and also improved power-on-reset circuitry for different application scenarios.

Three hardware pins (A0, A1 and A2) are used to program and vary the fixed I^2C address and allow up to 8 devices to share the same I^2C bus or SMBus.

8.2 Functional Block Diagram

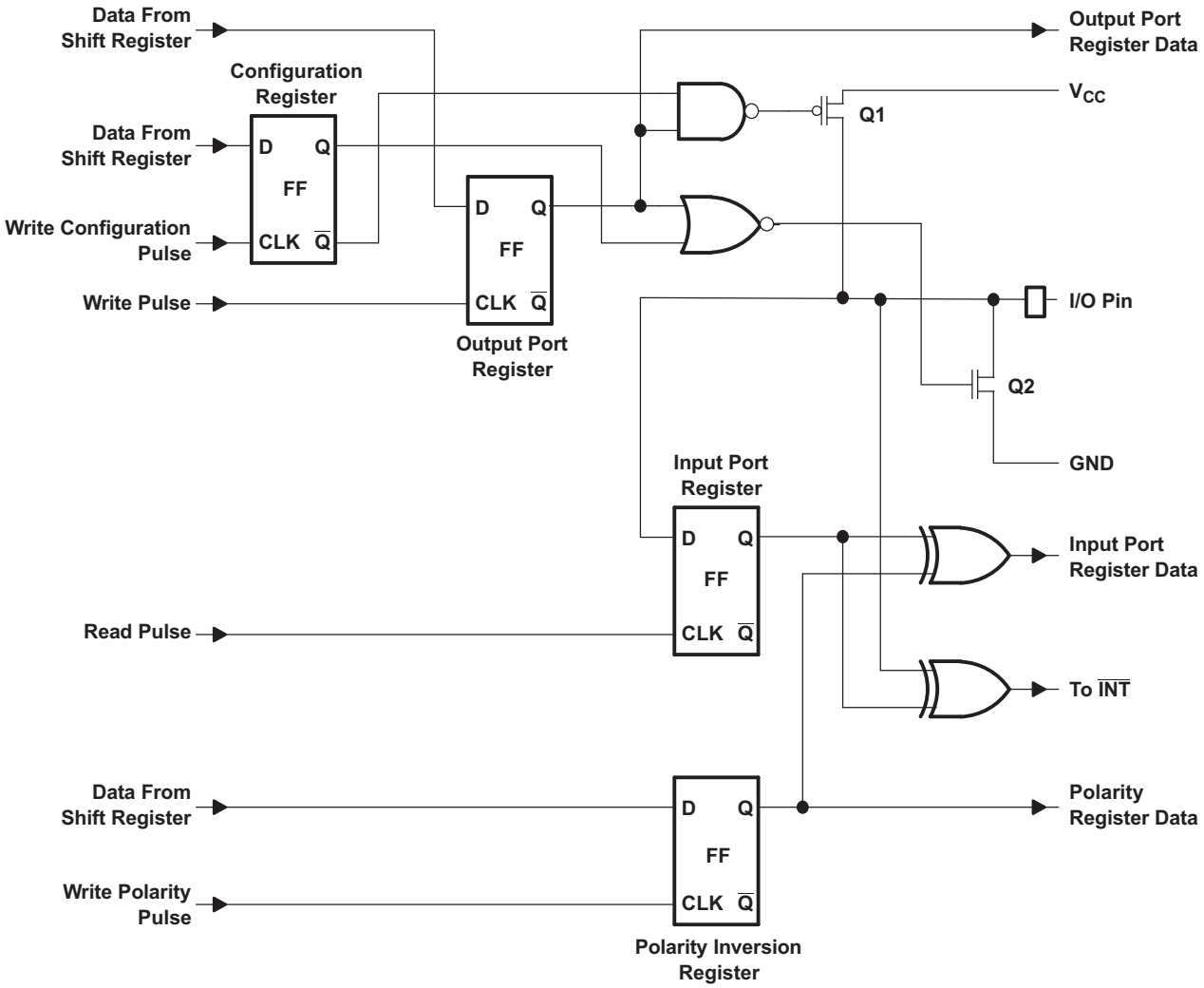


Pin numbers shown are for the PW package.

All I/Os are set to inputs at reset.

Figure 22. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)



At power-on reset, all registers return to default values.

Figure 23. Simplified Schematic of P-Port I/Os

8.3 Feature Description

8.3.1 5-V Tolerant I/O Ports

The TCA9535 device features I/O ports, which are tolerant of up to 5 V. This allows the TCA9535 to be connected to a large array of devices. To minimize I_{CC}, any input signals must be designed so that the input voltage stays within V_{IH} and V_{IL} of the device as described in the *Electrical Characteristics* section.

8.3.2 Hardware Address Pins

The TCA9535 features 3 hardware address pins (A0, A1, and A2) to allow the user to select the device's I^2C address by pulling each pin to either V_{CC} or GND to signify the bit value in the address. This allows up to 8 TCA9535 devices to be on the same bus without address conflicts. See the *Functional Block Diagram* to see the 3 address pins. The voltage on the pins must not change while the device is powered up in order to prevent possible I^2C glitches as a result of the device address changing during a transmission. All of the pins must be tied either to V_{CC} or GND and cannot be left floating.

Feature Description (continued)

8.3.3 Interrupt ($\overline{INT}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the $\overline{INT}$ is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. Because each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or vice versa.

$\overline{INT}$ has an open-drain structure and requires a pull-up resistor to V_{CC} of moderate value (typically about 10 kΩ).

8.4 Device Functional Modes

8.4.1 Power-On Reset (POR)

When power (from 0 V) is applied to V_{CC}, an internal power-on reset circuit holds the TCA9535 in a reset condition until V_{CC} has reached V_{PORR}. At that time, the reset condition is released, and the TCA9535 registers and I^2C-SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle.

8.4.2 Powered-Up

When power has been applied to V_{CC} above V_{PORR}, and the POR has taken place, the device is in a functioning mode. In this state, the device is ready to accept any incoming I^2C requests and is monitoring for changes on the input ports.

8.5 Programming

8.5.1 I^2C Interface

The TCA9535 has a standard bidirectional I^2C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I^2C bus has a specific device address to differentiate between other slave devices that are on the same I^2C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. For more information see *Understanding the I^2C Bus* application report, SLVA704.

The physical I^2C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I^2C lines. For further details, see *I^2C Pull-up Resistor Calculation* application report, SLVA689. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition. See Table 1.

Figure 24 and Figure 25 show the general procedure for a master to access a slave device:

1. If a master wants to send data to a slave:
   - Master-transmitter sends a START condition and addresses the slave-receiver.
   - Master-transmitter sends data to slave-receiver.
   - Master-transmitter terminates the transfer with a STOP condition.
2. If a master wants to receive or read data from a slave:
   - Master-receiver sends a START condition and addresses the slave-transmitter.
   - Master-receiver sends the requested register to read to slave-transmitter.
   - Master-receiver receives data from the slave-transmitter.

Programming (continued)

– Master-receiver terminates the transfer with a STOP condition.

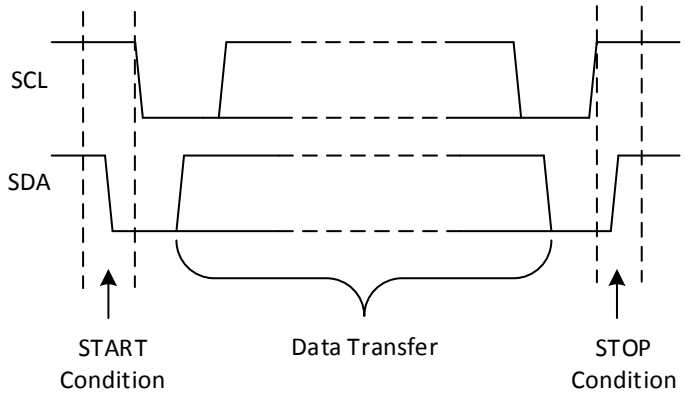


Figure 24. Definition of Start and Stop Conditions

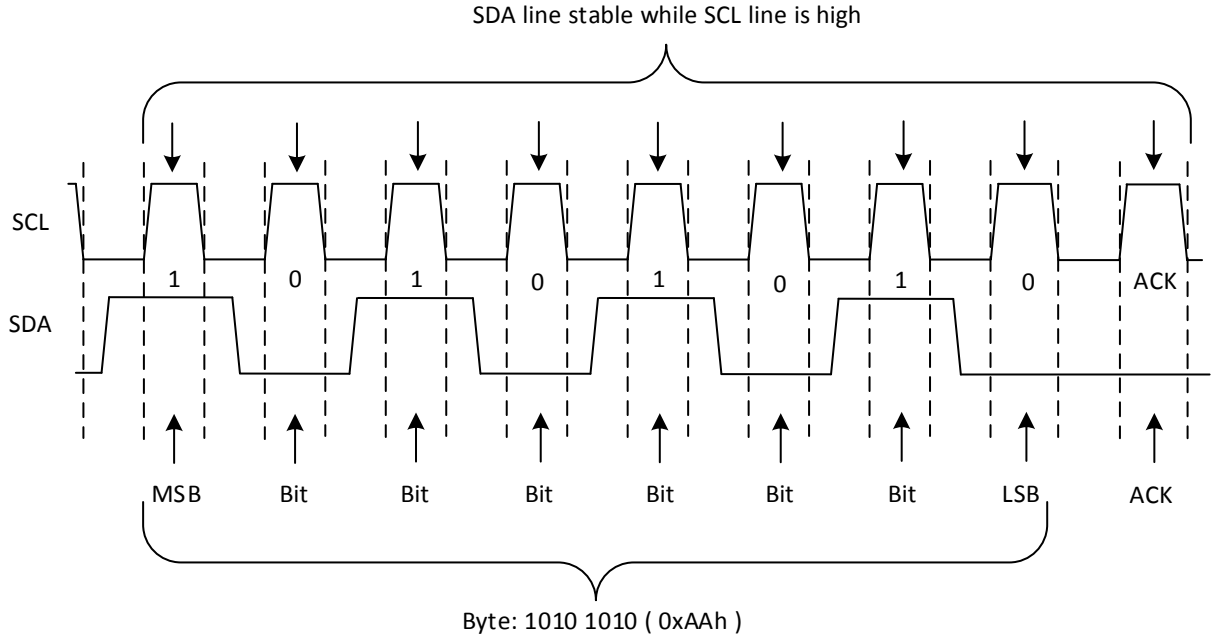


Figure 25. Bit Transfer

Table 1 shows the interface definition.

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

8.5.1.1 Bus Transactions

Data is exchanged between the master and the TCA9535 through write and read commands, and this is accomplished by reading from or writing to registers in the slave device.

Programming (continued)

Registers are locations in the memory of the slave which contain information, whether it be the configuration information or some sampled data to send back to the master. The master must write information to these registers in order to instruct the slave device to perform a task.

8.5.1.1.1 Writes

To write on the I^2C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/$\overline{W}$ bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master then sends the register address of the register to which it wishes to write. The slave acknowledges again, letting the master know it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

See the *Control Register and Command Byte* section to see list of the TCA9535's internal registers and a description of each one.

Figure 26 shows an example of writing a single byte to a slave register.

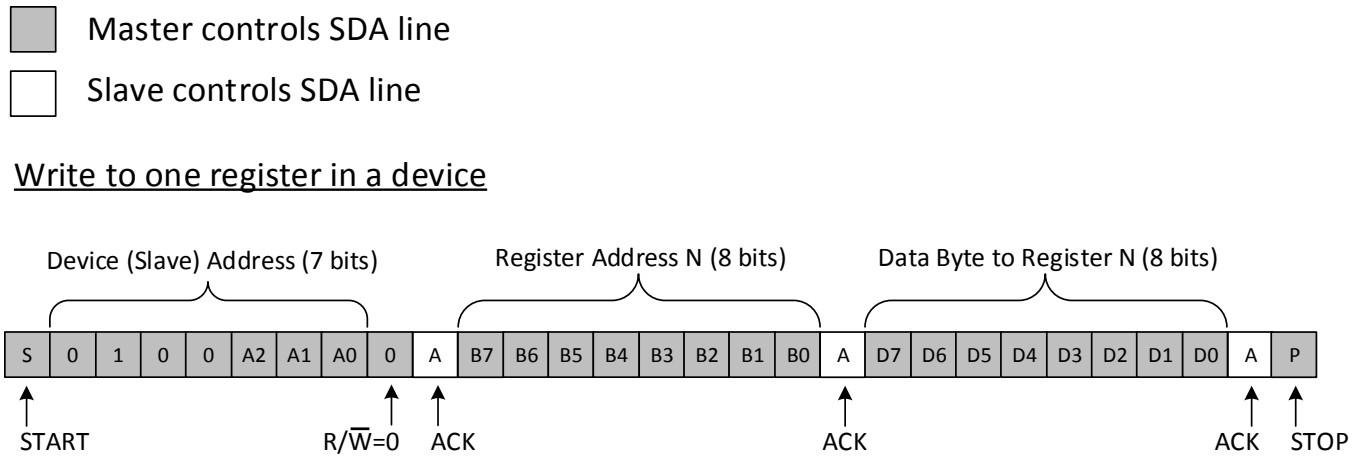


Figure 26. Write to Register

Figure 27 shows the Write to the Polarity Inversion Register.

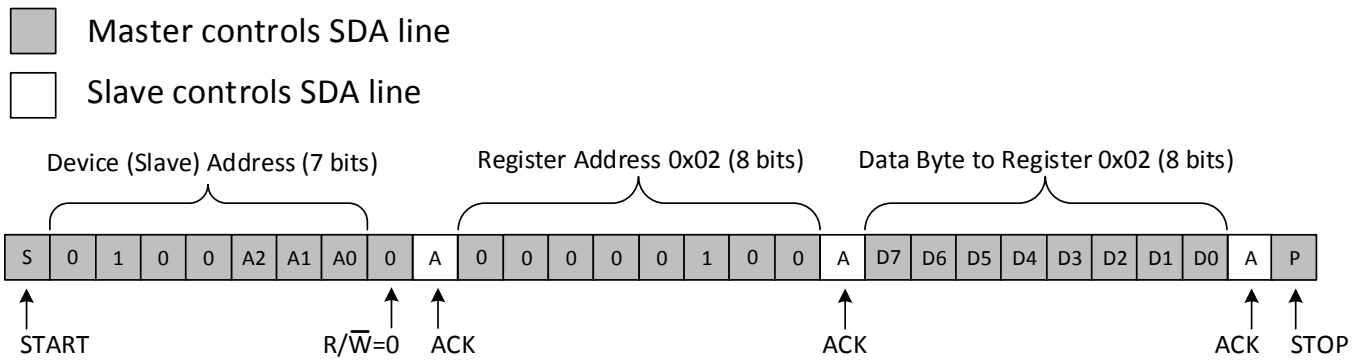


Figure 27. Write to the Polarity Inversion Register

Figure 28 shows the Write to Output Port Registers.

Programming (continued)

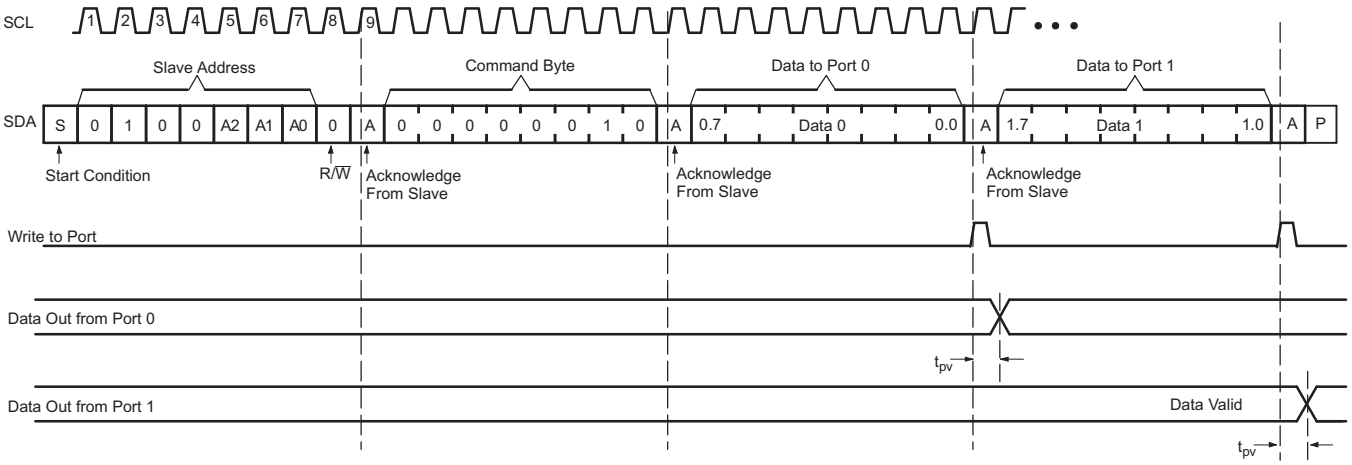


Figure 28. Write to Output Port Registers

8.5.1.1.2 Reads

Reading from a slave is very similar to writing, but requires some additional steps. In order to read from a slave, the master must first instruct the slave which register it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/$\overline{W}$ bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the slave acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/$\overline{W}$ bit set to 1 (signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmitter.

The master continues to send out the clock pulses, but releases the SDA line so that the slave can transmit data. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. When the master has received the number of bytes it is expecting, it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

See the *Control Register and Command Byte* section to see list of the TCA9535's internal registers and a description of each one.

Figure 29 shows an example of reading a single byte from a slave register.

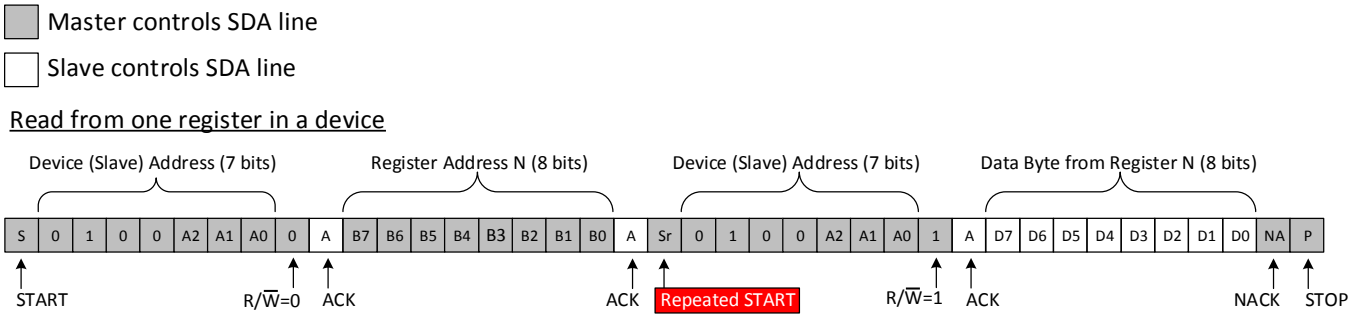
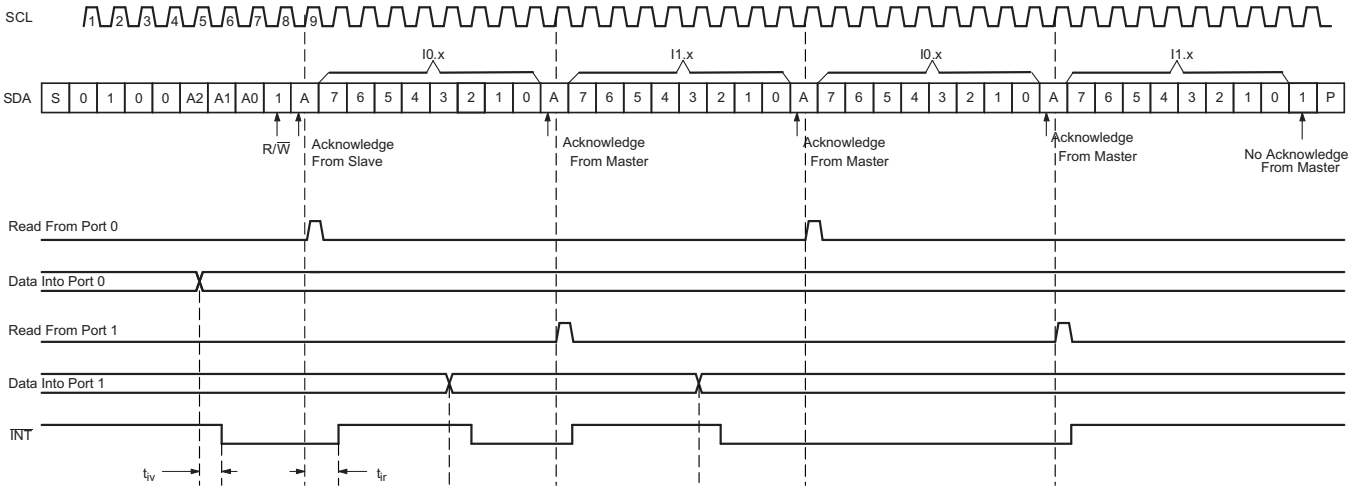


Figure 29. Read from Register

Programming (continued)

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data. Figure 30 and Figure 31 show two different scenarios of Read Input Port Register.

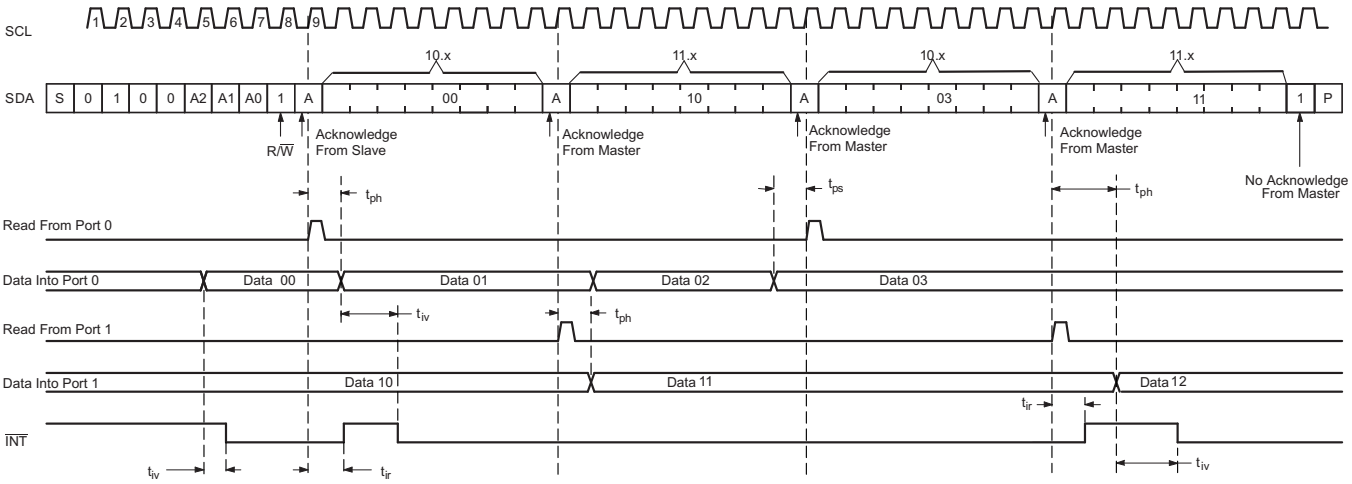


Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port.

Figure 30. Read Input Port Register, Scenario 1

Programming (continued)



Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port.

Figure 31. Read Input Port Register, Scenario 2

8.5.2 Device Address

Figure 32 shows the address byte of the TCA9535.

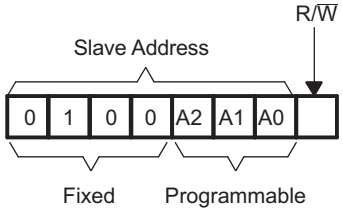


Figure 32. TCA9535 Address

Table 2 shows the address reference of the TCA9535.

Table 2. Address Reference

INPUTS			I^2C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 0×20 (hexadecimal)
L	L	H	33 (decimal), 0x21 (hexadecimal)
L	H	L	34 (decimal), 0x22 (hexadecimal)
L	H	H	35 (decimal), 0x23 (hexadecimal)
H	L	L	36 (decimal), 0x24 (hexadecimal)
H	L	H	37 (decimal), 0x25 (hexadecimal)
H	H	L	38 (decimal), 0x26 (hexadecimal)
H	H	H	39 (decimal), 0x27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.5.3 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte shown in Table 3 that is stored in the control register in the TCA9535. Three bits of this data byte state the operation (read or write) and the internal register (input, output, polarity inversion, or configuration) that is affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

When a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent. Figure 33 shows the control register bits.

0	0	0	0	0	B2	B1	B0

Figure 33. Control Register Bits

Table 3. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read-write byte	1111 1111
0	1	1	0x03	Output Port 1	Read-write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read-write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read-write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read-write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read-write byte	1111 1111

8.6 Register Maps

8.6.1 Register Descriptions

The Input Port registers (registers 0 and 1) shown in Table 4 reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I^2C device know that the Input Port registers are accessed next.

Table 4. Registers 0 and 1 (Input Port Registers)

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) shown in Table 5 show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Registers 2 and 3 (Output Port Registers)

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0

Table 5. Registers 2 and 3 (Output Port Registers) (continued)

Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) shown in Table 6 allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding pin's original polarity is retained.

Table 6. Registers 4 and 5 (Polarity Inversion Registers)

Bit	**N0.7**	**N0.6**	**N0.5**	**N0.4**	**N0.3**	**N0.2**	**N0.1**	**N0.0**
Default	0	0	0	0	0	0	0	0
Bit	**N1.7**	**N1.6**	**N1.5**	**N1.4**	**N1.3**	**N1.2**	**N1.1**	**N1.0**
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) shown in Table 7 configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 7. Registers 6 and 7 (Configuration Registers)

Bit	**C0.7**	**C0.6**	**C0.5**	**C0.4**	**C0.3**	**C0.2**	**C0.1**	**C0.0**
Default	1	1	1	1	1	1	1	1
Bit	**C1.7**	**C1.6**	**C1.5**	**C1.4**	**C1.3**	**C1.2**	**C1.1**	**C1.0**
Default	1	1	1	1	1	1	1	1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

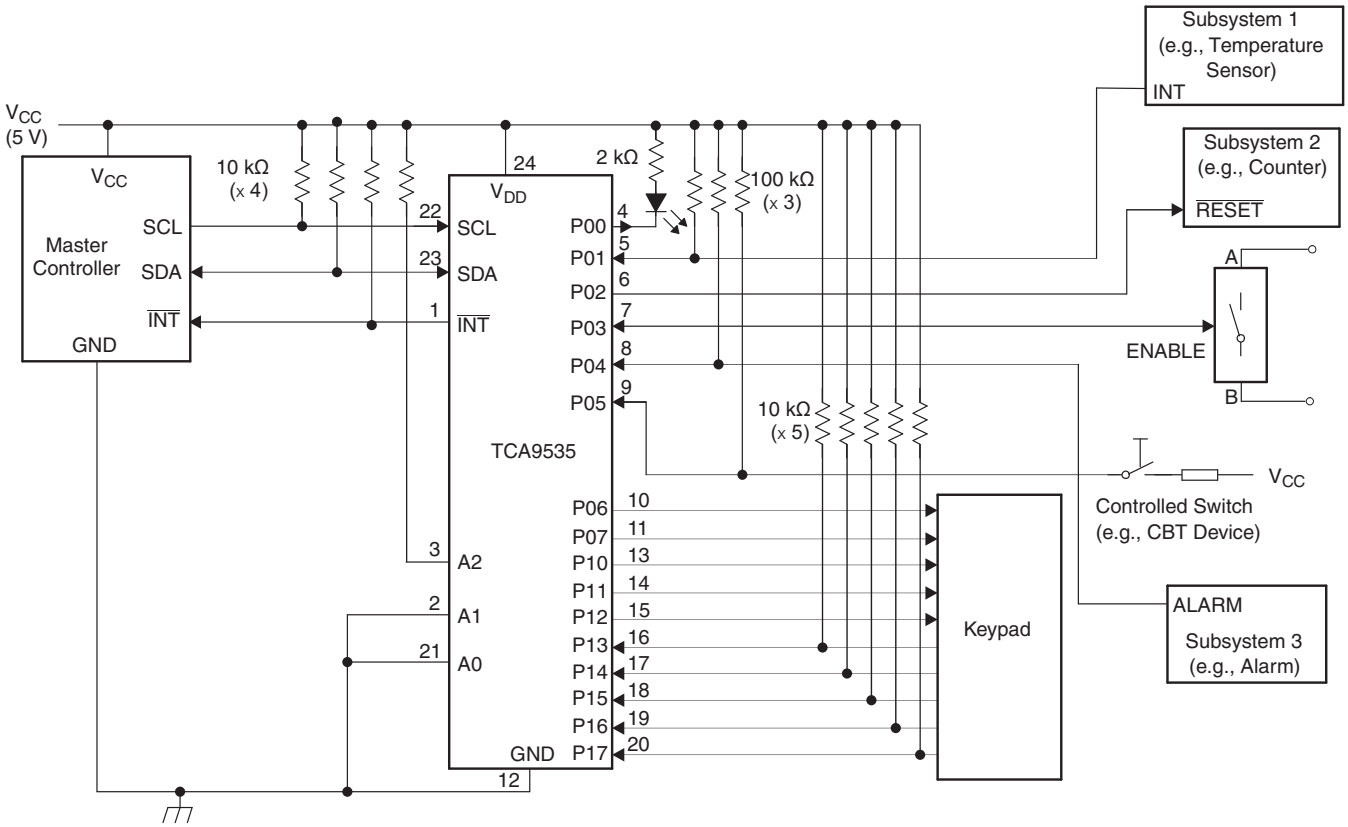
9.1 Application Information

Applications of the TCA9535 has this device connected as a slave to an I^2C master (processor), and the I^2C bus may contain any number of other slave devices. The TCA9535 is typically in a remote location from the master, placed close to the GPIOs to which the master needs to monitor or control.

IO Expanders such as the TCA9535 are typically used for controlling LEDs (for feedback or status lights), controlling enable or reset signals of other devices, and even reading the outputs of other devices or buttons.

9.2 Typical Application

Figure 34 shows an application in which the TCA9535 can be used.



Device address is configured as 0100100 for this example.

P00, P02, and P03 are configured as outputs.

P01, P04–P07, and P10–P17 are configured as inputs.

Pin numbers shown are for the PW package.

Figure 34. Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

The designer must take into consideration the system, to be sure not to violate any of the parameters. Table 8 shows some key parameters which must not be violated.

Table 8. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
I^2C and Subsystem Voltage (V_{CC})	5 V
Output current rating, P-port sinking (I_{OL})	25 mA
I^2C bus clock (SCL) speed	400 kHz

9.2.1.1 Calculating Junction Temperature and Power Dissipation

When designing with this device, it is important that the *Recommended Operating Conditions* not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in Equation 1.

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (1)$$

θ_{JA} is the standard junction to ambient thermal resistance measurement of the package, as seen in *Thermal Information* table. P_d is the total power dissipation of the device, and the approximation is shown in Equation 2.

$$P_d \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (2)$$

Equation 2 is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the $\overline{INT}$ and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using Equation 3 to calculate the power dissipation in $\overline{INT}$ or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (3)$$

Equation 3 shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the V_{OL} of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = (I_{OH} \times (V_{CC} - V_{OH})) \quad (4)$$

Equation 4 shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between V_{CC} and the output voltage).

9.2.1.2 Minimizing I_{CC} When I/O is Used to Control LED

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor as shown in Figure 34. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in the *Electrical Characteristics* table shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption.

Figure 35 shows a high-value resistor in parallel with the LED. Figure 36 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply current consumption when the LED is off.

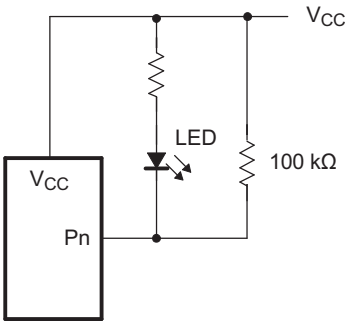


Figure 35. High-Value Resistor in Parallel With LED

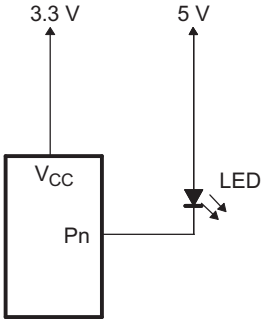


Figure 36. Device Supplied by Lower Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL} as shown in Equation 5.

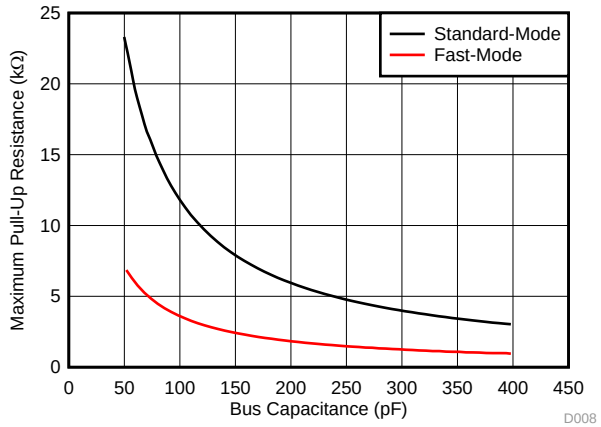
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (5)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b as shown in Equation 6.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (6)$$

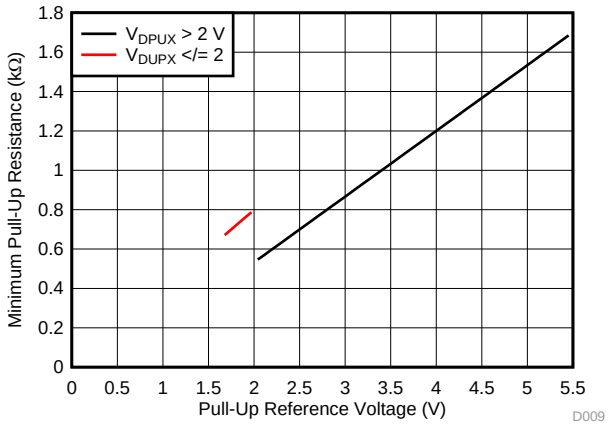
The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9538, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus. For further details, refer to *I^2C Pull-up Resistor Calculation* application report, SLVA689.

9.2.3 Application Curves



Standard-mode: f_{SCL} = 100 kHz, t_r = 1 µs
Fast-mode: f_{SCL} = 400 kHz, t_r = 300 ns

Figure 37. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2 × V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V
V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

Figure 38. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

10 Power Supply Recommendations

In the event of a glitch or data corruption, the TCA9535 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 39 and Figure 40.

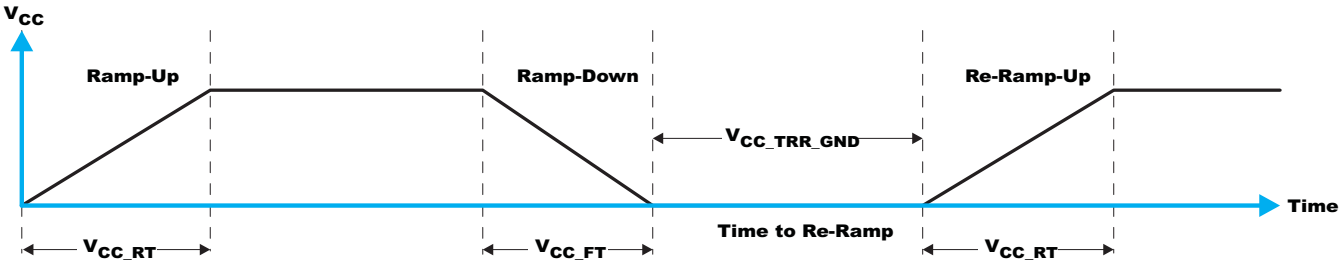


Figure 39. V_{CC} is Lowered Below 0.2 V or 0 V and then Ramped Up to V_{CC}

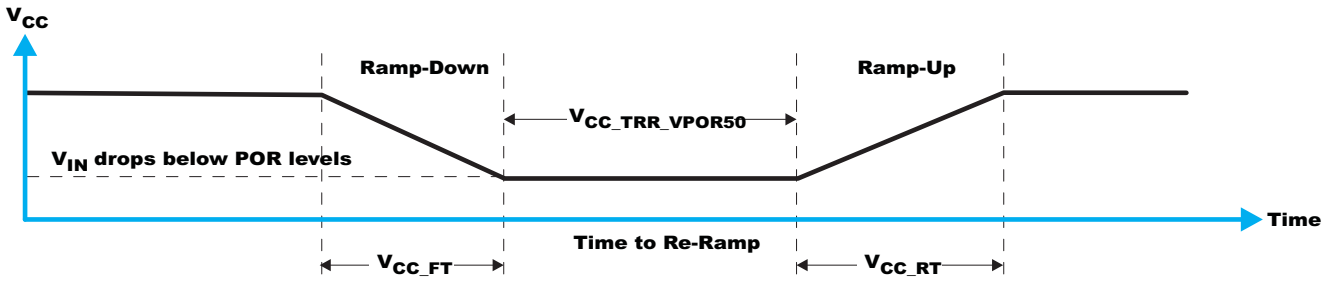


Figure 40. V_{CC} is Lowered Below the POR Threshold, then Ramped Back Up to V_{CC}

Table 9 specifies the performance of the power-on reset feature for TCA9535 for both types of power-on reset.

Table 9. Recommended Supply Sequencing and Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 40	0.1			ms
V_{CC_RT}	Rise rate	See Figure 40	0.1			ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV or when V_{CC} drops to GND)	See Figure 40	1			µs
V_{CC_GH}	The level (referenced to V_{CC}) that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW}	See Figure 41			1.2	V
V_{CC_MV}	The minimum voltage that V_{CC} can glitch down to without causing a reset (V_{CC_GH} must not be violated)	See Figure 41	1.5			V
V_{CC_GW}	Glitch width that does not cause a functional disruption	See Figure 41			10	µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.75	1		V
V_{PORR}	Voltage trip point of POR on rising V_{CC}			1.2	1.5	V

(1) T_A = –40°C to +85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 41 and Table 9 provide more information on how to measure these specifications.

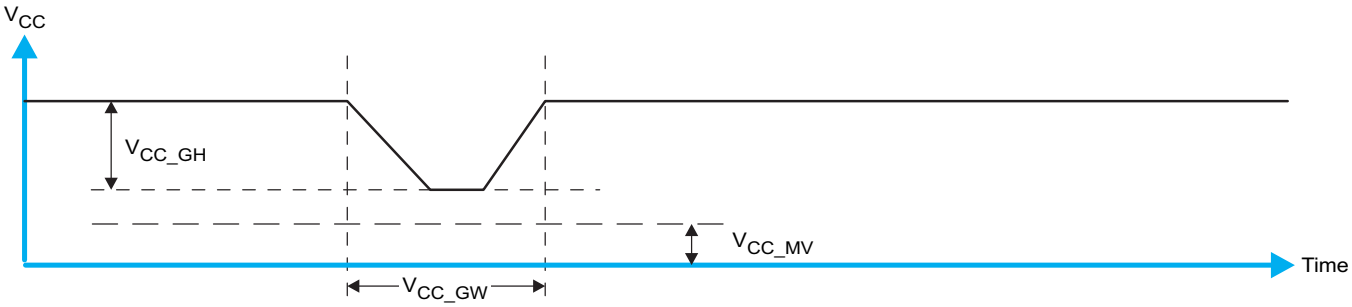


Figure 41. Glitch Width and Glitch Height

V_{PORR} is critical to the power-on reset. V_{PORR} is the voltage level at which the reset condition is released and all the registers and the I^2C-SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 42 and Table 9 provide more details on this specification.

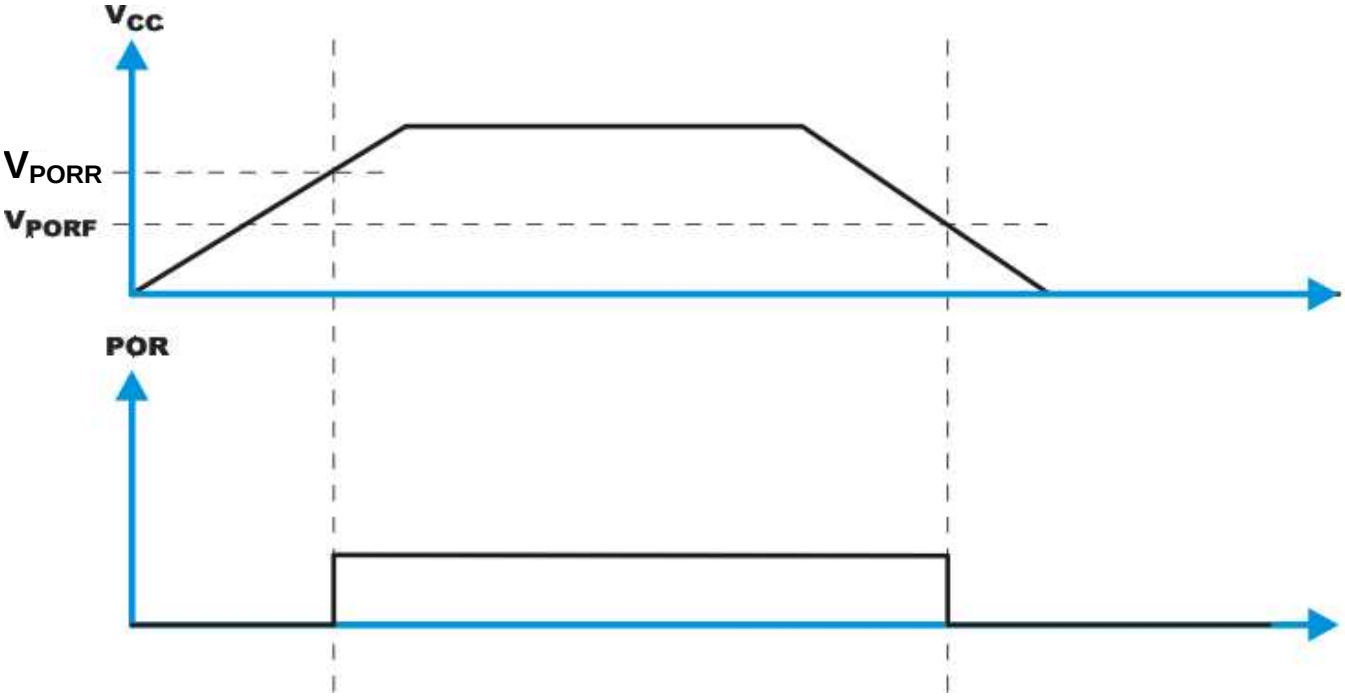


Figure 42. V_{POR}

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9535, common PCB layout practice must be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CC} pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9535 as possible. These best practices are shown in the *Layout Example*.

For the layout example provided in the *Layout Example*, it must be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC}, or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in the *Layout Example*.

11.2 Layout Example

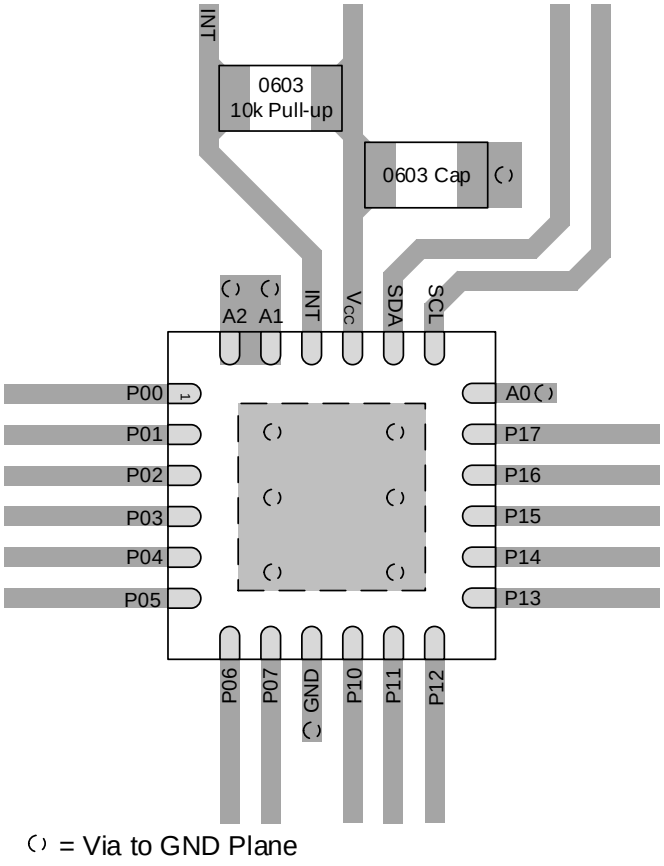


Figure 43. TCA9535 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *I2C Bus Pull-Up Resistor Calculation*, SLVA689
- *Maximum Clock Frequency of I2C Bus Using Repeaters*, SLVA695
- *Introduction to Logic*, SLVA700
- *Understanding the I2C Bus*, SLVA704
- *IO Expander EVM User's Guide*, SLVUA59A

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9535DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD9535	Samples
TCA9535DBT	ACTIVE	SSOP	DB	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD9535	Samples
TCA9535MRGER	PREVIEW	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TD9535	
TCA9535PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW535	Samples
TCA9535RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TD9535	Samples
TCA9535RTWR	ACTIVE	WQFN	RTW	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW535	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

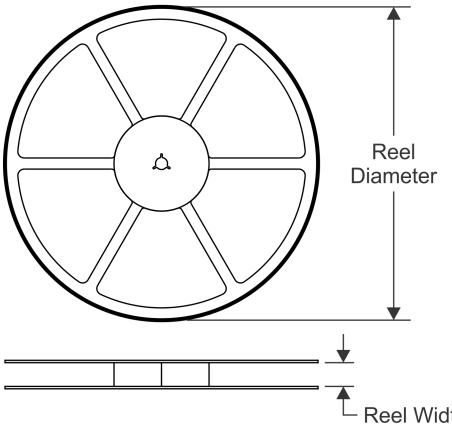
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

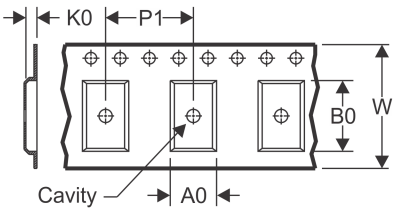
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

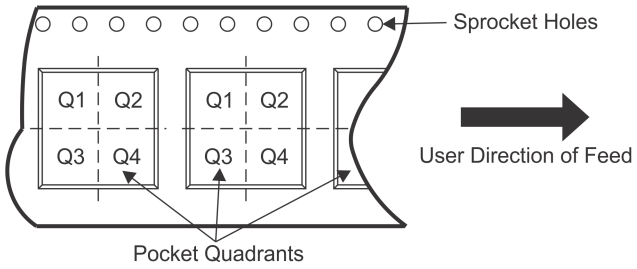


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

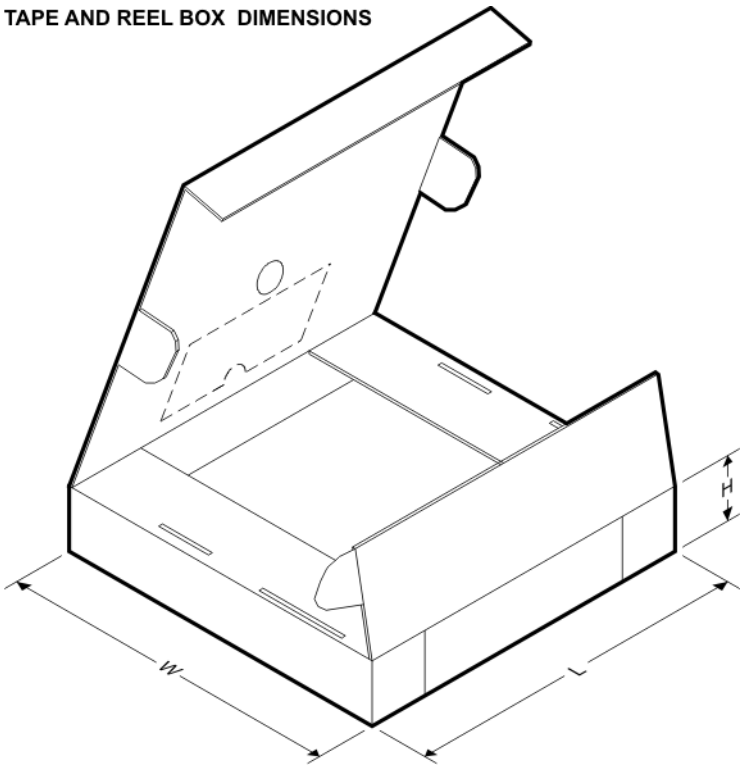
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9535DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
TCA9535DBT	SSOP	DB	24	250	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
TCA9535PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCA9535RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TCA9535RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

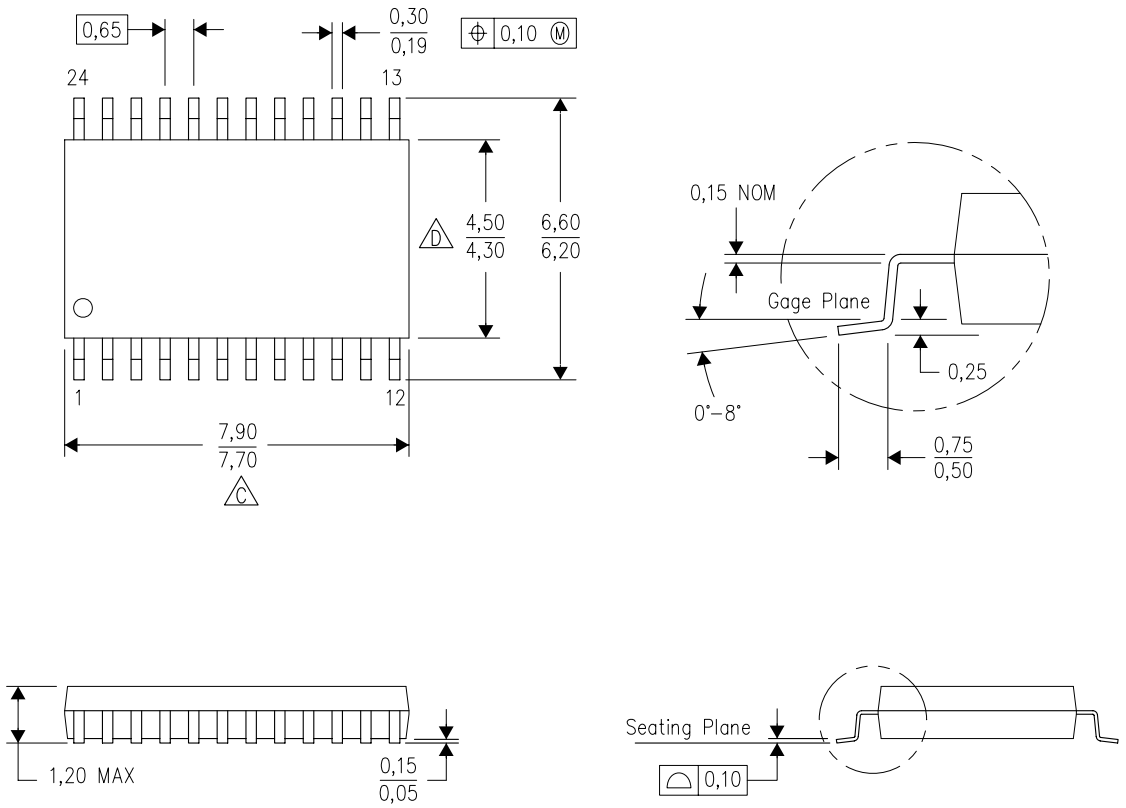
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9535DBR	SSOP	DB	24	2000	367.0	367.0	38.0
TCA9535DBT	SSOP	DB	24	250	367.0	367.0	38.0
TCA9535PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
TCA9535RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TCA9535RTWR	WQFN	RTW	24	3000	367.0	367.0	35.0

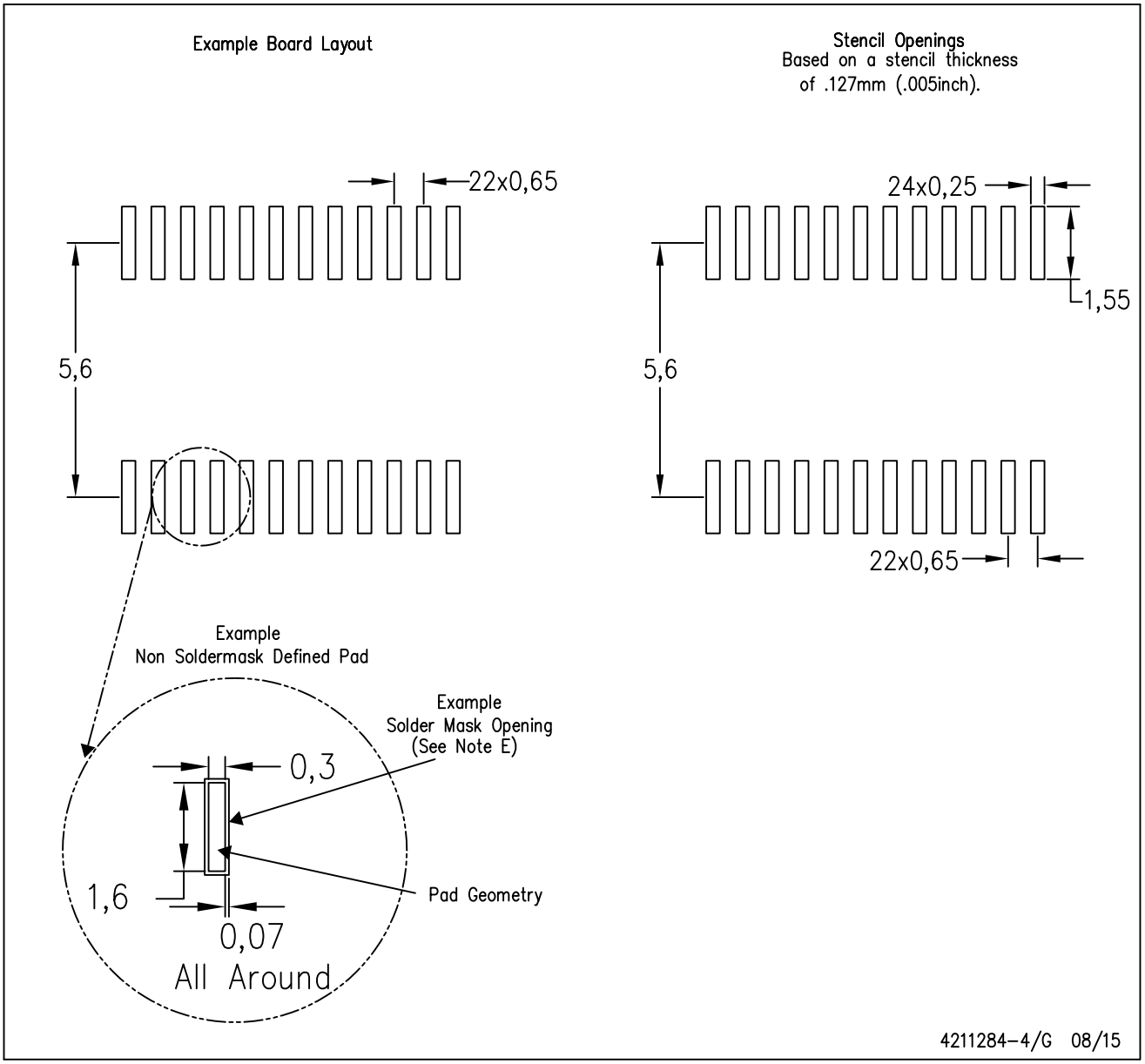
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

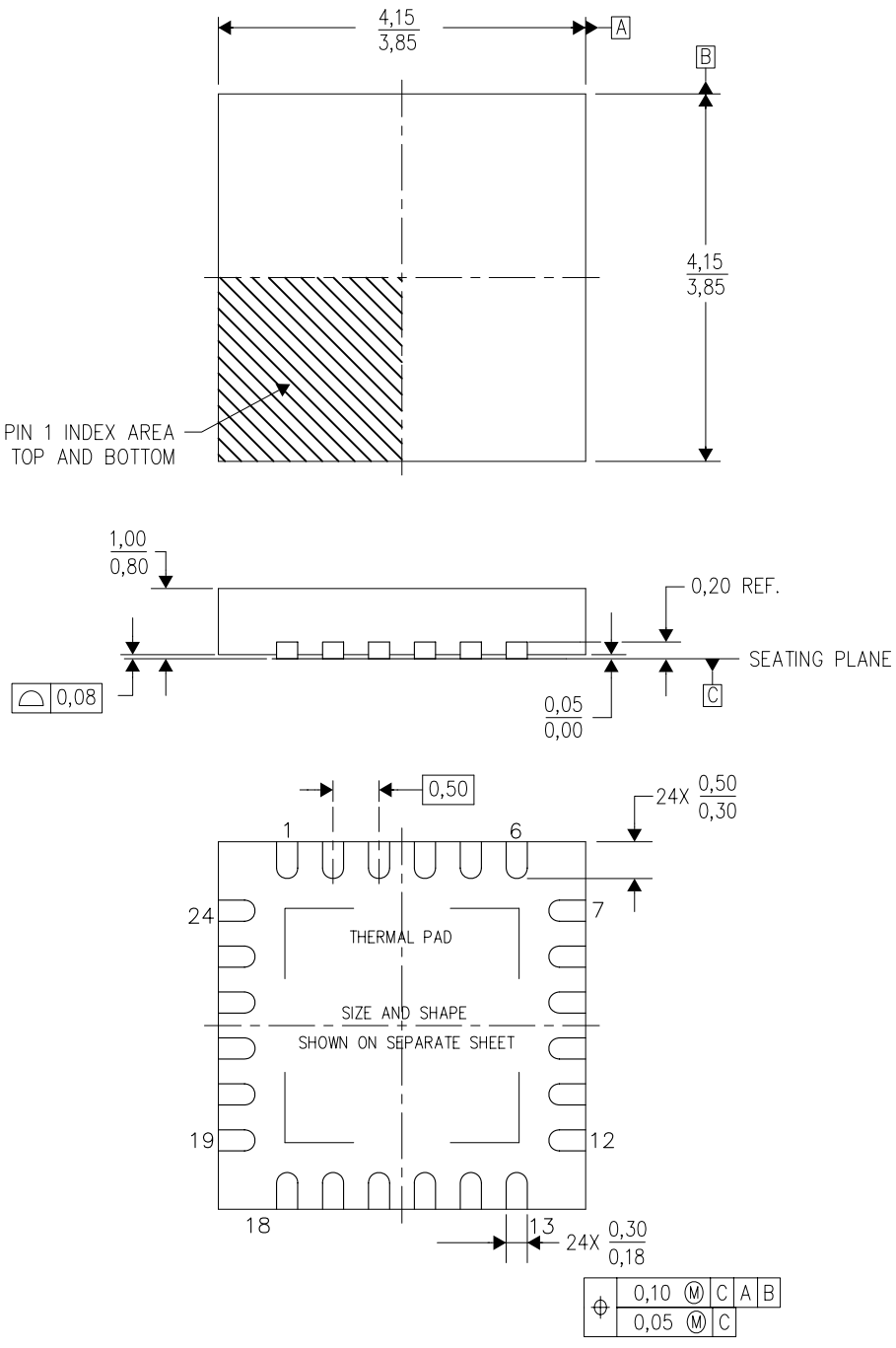
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

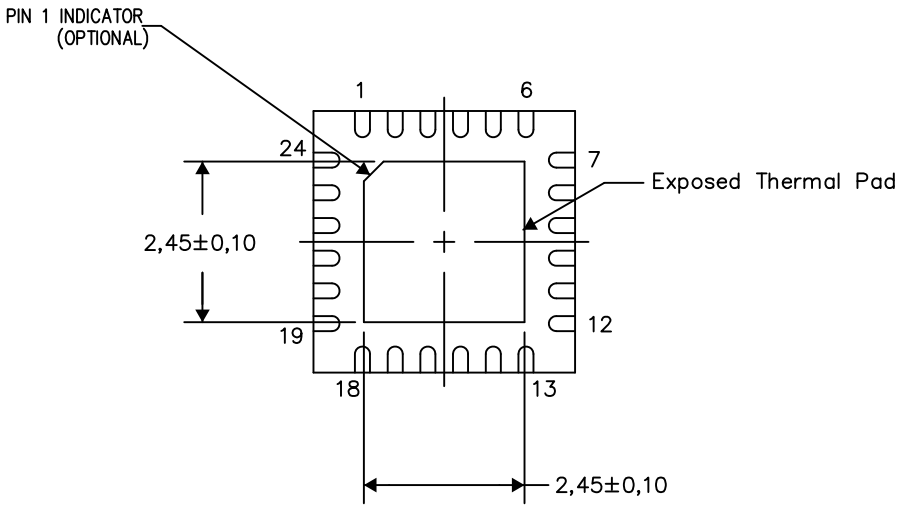
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



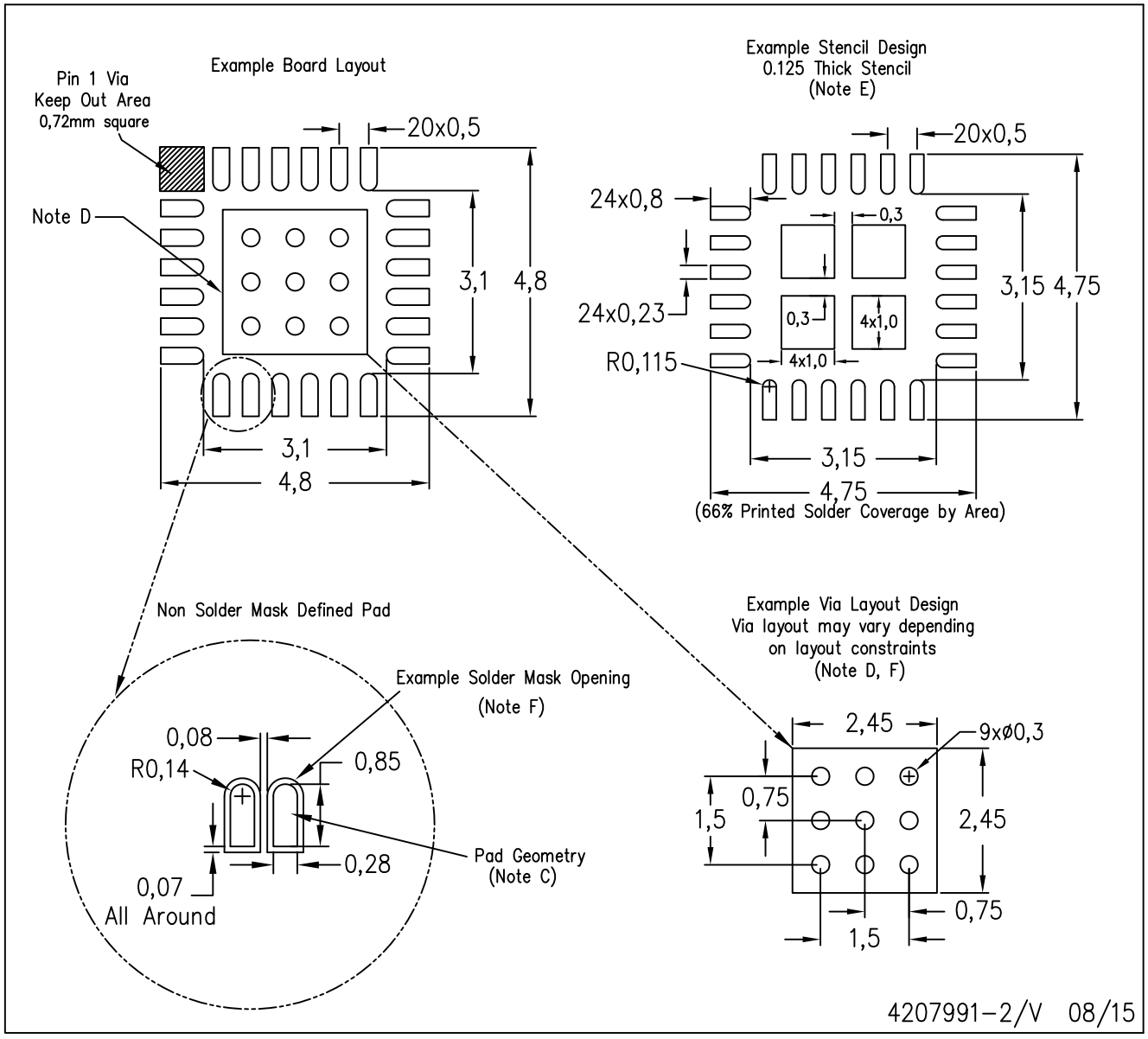
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

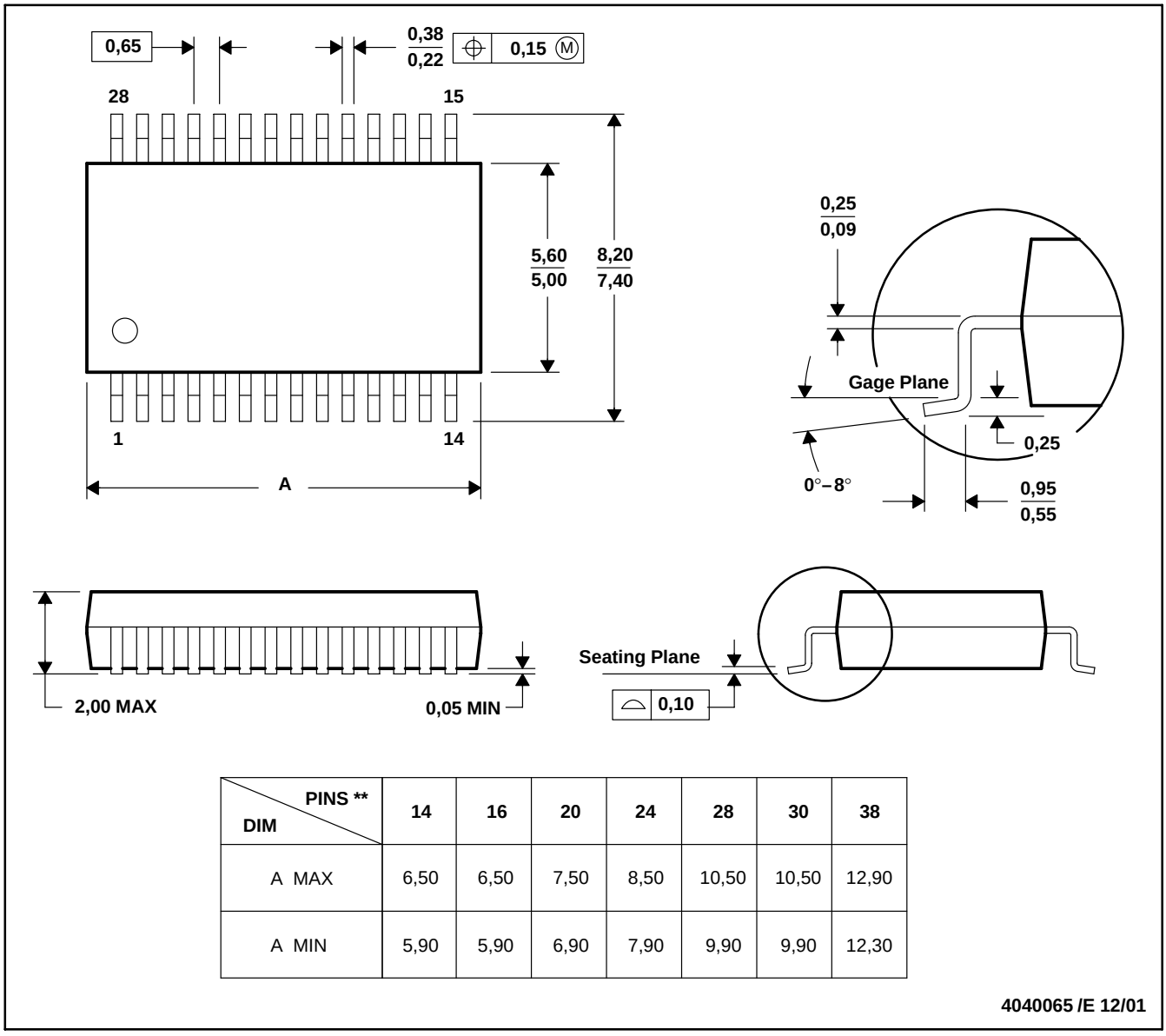


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

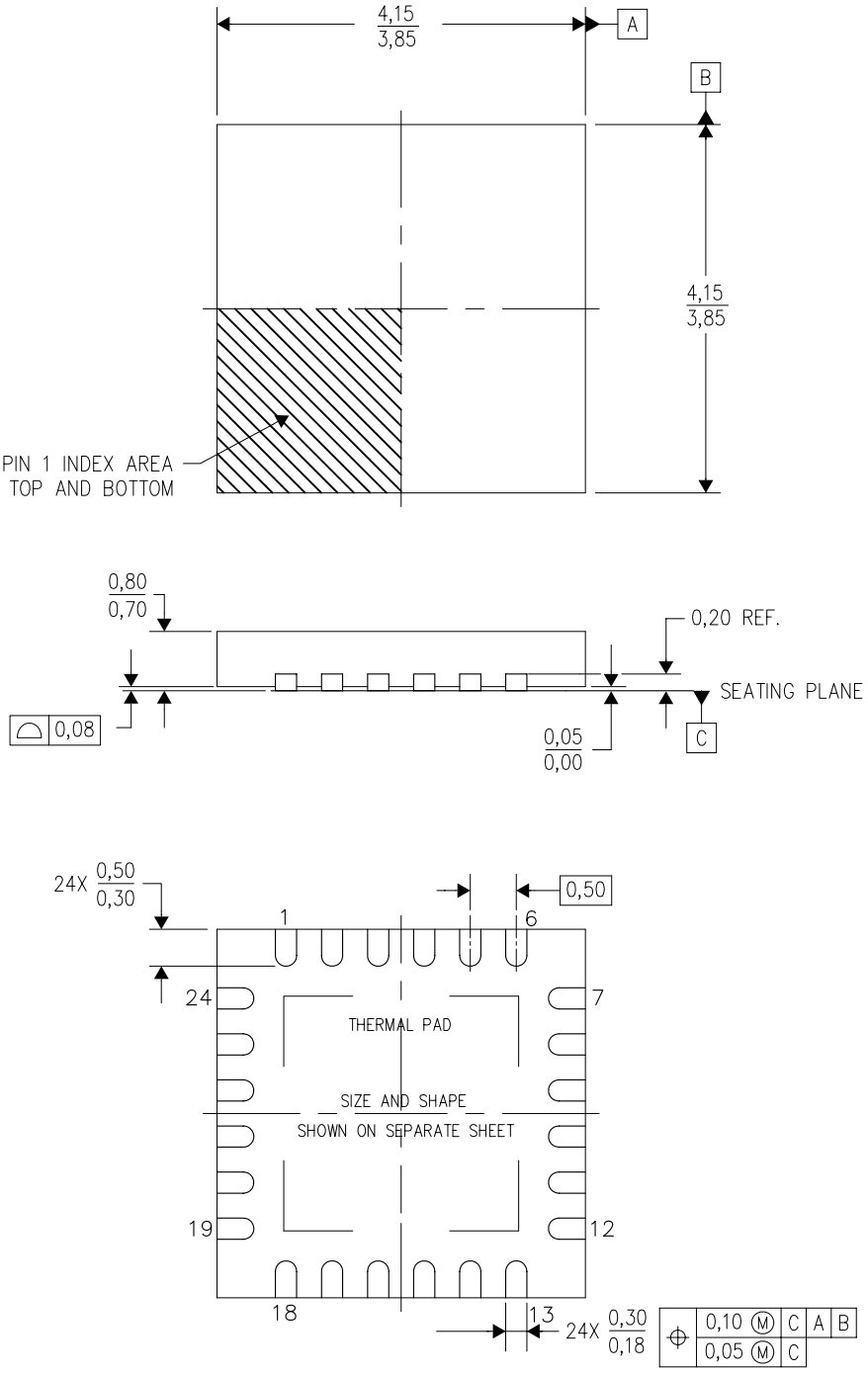


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

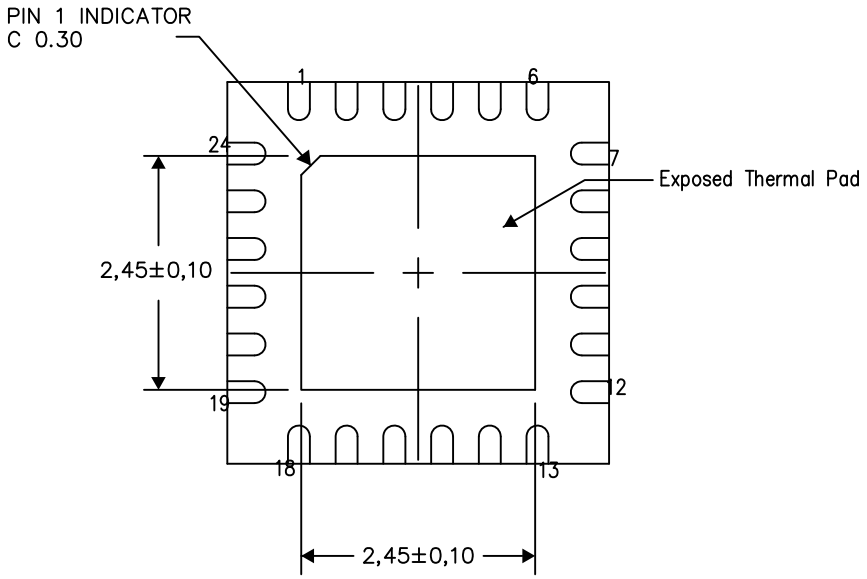
RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



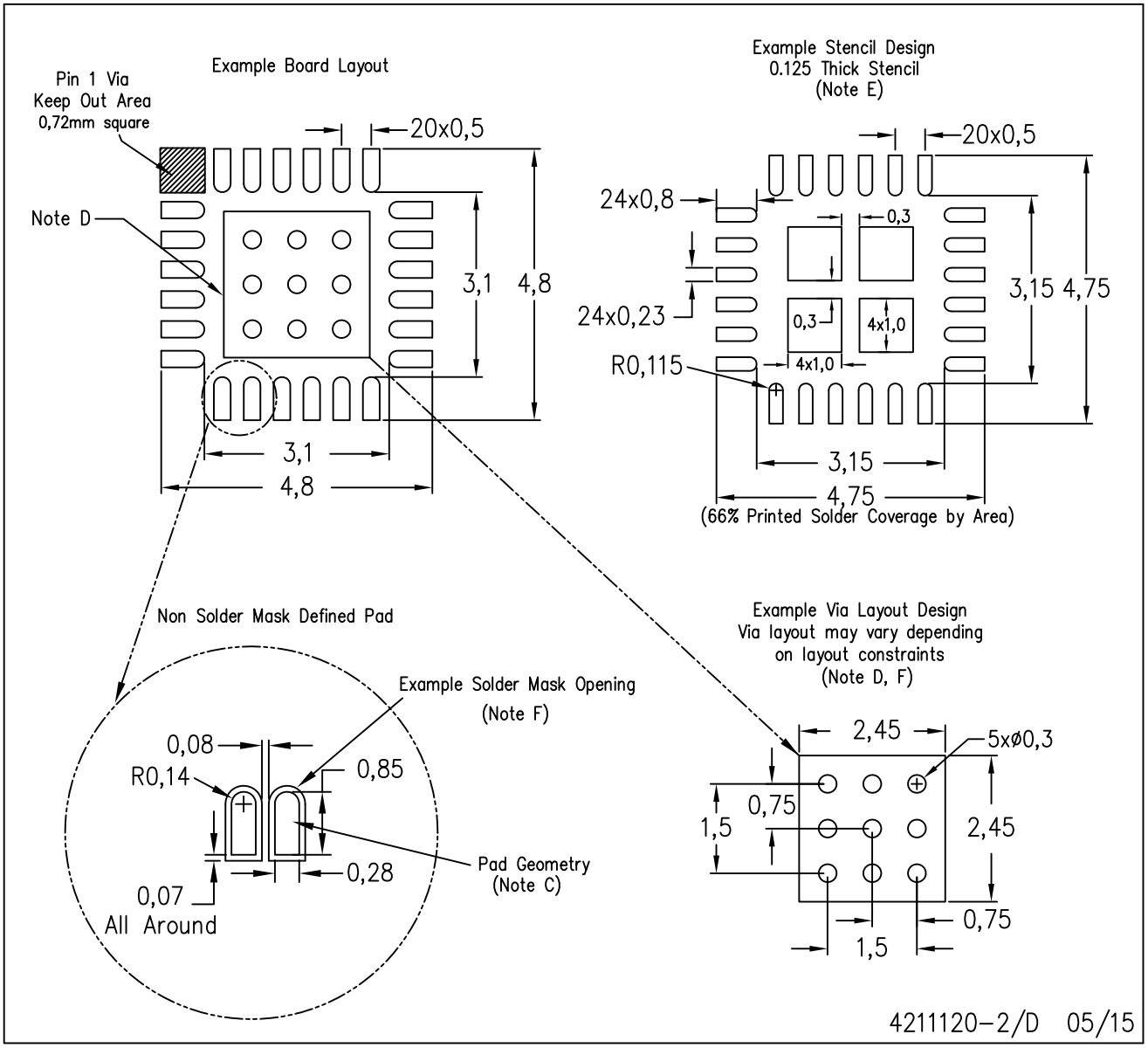
Bottom View

Exposed Thermal Pad Dimensions

4206249–3/P 05/15

NOTES: A. All linear dimensions are in millimeters

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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